MODEL 56100A
SCALAR NETWORK ANALYZER

MAINTENANCE MANUAL

Anritsu

490 JARVIS DRIVE ● MORGAN HILL, CA 95037-2809

P/N: 10410-00195
REVISION: C
PRINTED: OCTOBER 1997
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DECLARATION OF CONFORMITY

Manufacturer's Name: ANRITSU COMPANY

Manufacturer's Address: Microwave Measurements Division
490 Jarvis Drive
Morgan Hill, CA 95037-2809
USA

declares that the product specified below:

Product Name: Scalar Network Analyzers

Model Number: 56100A

conforms to the requirement of:

EMC Directive 89/336/EEC as amended by Council Directive 92/31/EEC & 93/68/EEC
Low Voltage Directive 73/23/EEC as amended by Council directive 93/68/EEC

Electromagnetic Interference:

Emissions:	CISPR 11:1990/EN55011:1991 Group 1 Class A
Immunity:	IEC 1000-4-2:1995/prEN50082-1:1995 - 4kV CD, 8kV AD IEC 1000-4-3:1993/ENV50140:1994 - 3V/m IEC 1000-4-4:1995/prEN50082-1:1995 - 0.5kV SL, 1kV PL IEC 1000-4-5:1995/prEN50082-1:1995 - 0.5kV - 1kV LN 0.5kV - 1kV NG 0.5kV - 1kV GL

Electrical Safety Requirement:

Product Safety:	IEC 1010-1:1990 + A1/EN61010-1:1993

Jon Blasi
Manager of Corporate Quality

Morgan Hill, CA

5-SEPT-97
Date

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Chapter 1
General Information

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Figure 1-1. *56100A Scalar Network Analyzer*

NOTE: ANRITSU Company was formerly known as WILTRON Company.

Chapter 1
General Information

1-1 SCOPE OF THE MANUAL

This manual provides general information, performance verification, calibration, parts lists, and service information for the ANRITSU Model 56100A Scalar Network Analyzer. The Model 56100A is shown in Figure 1-1.

1-2 INTRODUCTION

This Section provides a general description of the equipment, the unit identification number, other related manuals, performance specifications, and instrument options, exchange assembly program, static handling procedures, and recommended test equipment.

1-3 IDENTIFICATION NUMBER

All ANRITSU instruments are assigned a unique six-digit ID number, such as K 701001. Each 56100A has an ID number affixed to the outside of the rear panel. Please use this number when ordering parts or corresponding with ANRITSU's Customer Service department.

1-4 RELATED MANUALS

This manual is one of a two manual set that consists of an Operating and Programming Manual (OPM) and a Maintenance Manual (MM). The ANRITSU part number for this manual is listed on the title page.

1-5 ONLINE MANUAL

This manual is available on CD ROM as an Adobe Acrobat™ (*.pdf) file. The file can be viewed using Acrobat Reader™, a free program that is also available on the CD ROM. This file is "linked" such that the viewer can choose a topic to view from the displayed "bookmark" list and "jump" to the manual page on which the topic resides. The text can also be word-searched. Contact ANRITSU Customer Service for price and availability.

1-6 NETWORK ANALYSIS DESCRIPTION

Network analysis consists of the characterization of microwave devices through the measurement of the device transmission and impedance characteristics as a function of frequency. It includes the measurement of input match, output match, forward transmission, and reverse transmission. Each of these parameters is a complex quantity consisting of magnitude and phase.

A network analyzer system consists of three main elements: the signal source, the measurement components, and the network analyzer or signal processing element. There are two basic types of network analyzers: scalar and vector. Scalar network analyzers (SNAs) measure only the magnitude of the transmission or reflection signal. Vector network analyzers measure the magnitude and the phase of the transmission or reflection parameter. The 56100A is of the scalar network analyzer type.

1-7 56100A SCALAR NETWORK ANALYZER DESCRIPTION

The Model 56100A is a scalar network analyzer that has a frequency range of 10 MHz to 110 GHz, depending on the external test components and frequency sources used. (An external signal source is required for operation of this unit.) The Model 56100A is ideal for both production and R&D applications.

Measurement System Overview

With the addition of a programmable signal source, the 56100A becomes an automated transmission, return loss (SWR), and power measurement system. For example, with the appropriate test components and an ANRITSU 68169B frequency source, the 56100A will operate over the 10 MHz to 40 GHz range from a single coaxial test port. The 56100A

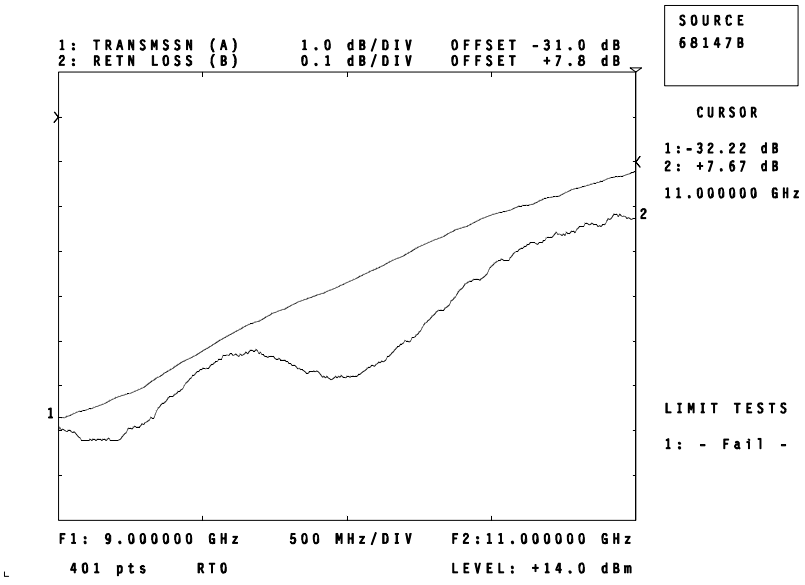


Figure 1-2. *Typical 56100A Annotated Display*

provides fully annotated displays of test data and measurement parameters as shown in Figure 1-2.

Under internal microprocessor control (no external controller required), the 56100A normalizes and simultaneously displays any two signals that are input on channels A, B, R1, and R2. The same inputs can be displayed as ratios A/R1, A/R2, B/R1, or B/R2. Depending on the external components used, the dynamic range for each channel is typically 76 dB (–60 dBm to +16 dBm). The noise floor is typically less than –62 dBm, providing a 76 dB (or greater) dynamic range for most applications.

Key 56100A features include:

- Automatic measurements and hard copy output without a controller.
- Accurate coaxial measurements from 10 MHz to 50 GHz.
- Nine stored setups to eliminate set-up time.
- Cursors, markers, and limit lines to improve productivity.
- Complete, annotated, step-by-step normalization and measurement procedures.
- Four measurement channels.
- Low cost.

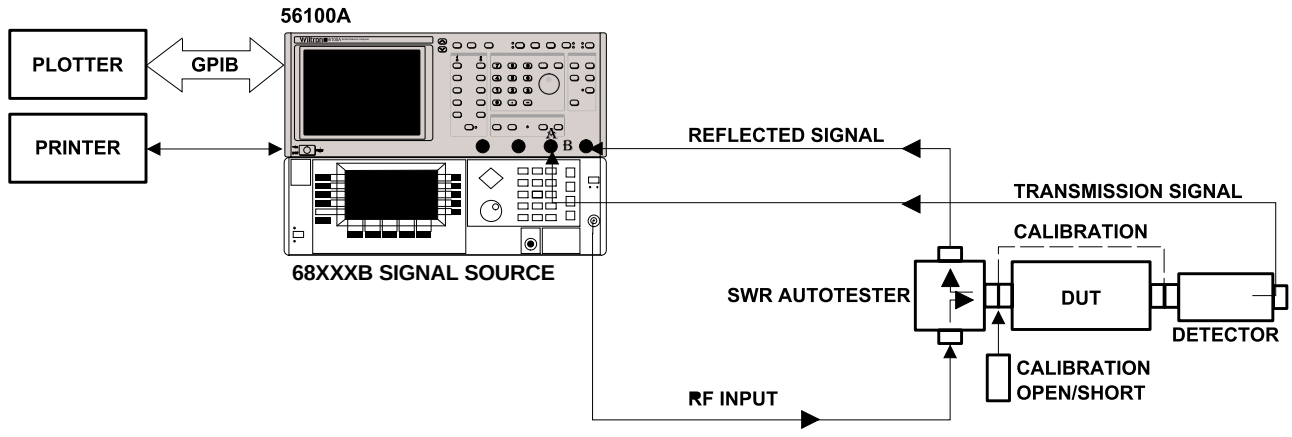


Figure 1-3. *Typical 56100A Test Setup*

Normalization and Measurement

In a typical 56100A test setup, the test device is inserted between the SWR Autotester and the detector (refer to Figure 1-3). Detected signals from the SWR Autotester vary in proportion to the reflections, while the detector output varies in proportion to transmission loss or gain. The detector can be used to measure power in dBm.

During normalization, procedural guidance is automatically provided for transmission and return loss measurements. For a return loss test, a 0 dB reference is established by connecting an open, then a short, to the SWR Autotester test port. The normalization data are taken independent of sensitivity settings at the number of points selected, with 0.002dB resolution, and stored in memory for correction of test data or for recall. Furthermore, an algorithm interpolates between data points to hold interpolated test data accuracy usually to within ±0.1 dB. Once the 56100A has been normalized across a user-selected frequency range, measurements can be made over any portion of the range without renormalization. Set-up time is greatly reduced by storing parameters for up to nine test setups for later reuse.

During measurements, data is taken at 101, 201, or 401 points (user selected) with 0.002 dB vertical resolution on both channels. Typically, test data is updated every 100 ms, allowing "real time" adjustments of the test device. A permanent record of the test data – with or without the test, marker, or stored setup parameters – is made automatically using an HP 7440A, 7470A, or 7475A plotter. Most dot-matrix printers may also be used, including the the Cannon BJ30 Bubble Jet Printer. Since the 56100A requires only about 10 seconds for print formatting, a new test can be conducted while the previously taken data is being printed out.

The 56100A is equally effective when used for waveguide reflectometer setups, where ratio measurements may be preferred. The 560-10BX-1 Adapter Cables provide the interface between the instrument and waveguide detectors.

Cursors, Markers, and Limit Lines

The 56100A has an extensive number of cursor functions available. These cursor functions are in addition to markers available when an ANRITSU 6600B, 6700A/B, or 68XXXB series signal generator is used as the system signal source. The 56100A communicates with the signal source through a dedi-

cated GPIB link and displays an identifier for each marker.

To speed the interpretation of data, complex limit lines can be entered by the user via the front panel keys or via the GPIB interface. Limit lines may have up to ten segments that may slope or step with frequency. Each segment of the limit line is numerically identified during entry.

Averaging and Smoothing

When characteristics of the test device vary rapidly with frequency at very low signal levels, the trace can be smoothed by use of the averaging and/or smoothing functions. The smoothing control has three selections: Off, Min, and Max. To maintain the accuracy of the measurement data, smoothing is performed by reducing bandwidth, rather than by averaging adjacent data points in order to preserve measurement detail.

When averaging is selected, 2 to 256 successive traces can be averaged to smooth the trace display. As various combinations of smoothing and averaging are selected, the trace update time is automatically adjusted.

Measurement Accuracy

The return-loss accuracy of the 56100A is largely attributable to the high directivity of the ANRITSU SWR Autotesters. For example, the 560-97A50-1 Autotester with its GPC-7 test port connector has a directivity of better than 40 dB from 10 MHz to 18 GHz. The 560-98K50 has a directivity that exceeds 35 dB up to 18 GHz, 32 dB up to 26.5 GHz, and 30 dB up to 40 GHz. The same unit has a test port match of better than 23 dB up to 26.5 GHz and 15 dB up to 40 GHz. To avoid the use of error-producing adapters, SWR autotesters are available with either male or female test ports in Type N, WSMA, or K connectors. All have high directivity. When the GPC-7 test port is selected, the lowest reflection adapters obtainable are offered in Type N and WSMA, which is optimized for testing SMA devices.

The accuracy of a transmission loss, gain, or power measurement is affected by reflections from the test port, the device under test, and the detector. These errors are minimized by the very low reflections from the ANRITSU SWR autotesters and detectors.

Zero-biased Schottky diodes are used in all 560-7xxx series detectors to minimize drift and circuit complexity. With the exception of the 560-7K50, the diode modules of these units are field-replaceable. This eliminates the expense and inconvenience of returning the detectors to a service center for repair.

The accuracy of the 56100A is high also because modulation of the input signal is not required. The need for modulation is avoided by using self-balancing amplifiers, which are stable at low signal levels. As a result, errors from modulation asymmetry and modulation-sensitive test devices are nonexistent. Without the insertion loss of a modulator, measurements can be made at higher input levels. This increases the measurement dynamic range.

Recommended Signal Sources

There are many advantages in selecting an ANRITSU 6600B, 6700A/B, or 68XXXB series signal source for use with the 56100A. One advantage is the power sweep. In this mode, the output power is swept over a 15 dB range, which enhances gain compression measurements. In the alternate sweep mode, the 56100A can display frequency response over different frequency ranges and/or power levels.

Another advantage of using ANRITSU signal sources is that they use fundamental oscillators from 2 to 20 GHz, thus avoiding the serious errors introduced by the subharmonics of frequency multipliers.

Stored Test Configuration Setups

Set-up time is reduced substantially by storing up to nine front-panel setups, four of which include the associated calibration data. A unique preview feature allows stored setup parameters to be reviewed before recalling or storing a new setup in the memory location. The stored data are backed by a battery with an estimated 5-year life.

GPIB Compatibility

The implementation of the IEEE-488 General Purpose Interface Bus (GPIB) is standard on the 56100A and provides remote control of all front-panel functions except power on/off and CRT intensity. A high speed data transfer mode can be used to transfer measurement data to the host computer; this capability is especially useful in manufacturing environments where archiving of data is required.

1-8 OPTIONS

The following standard instrument option is available:

Option 1, Rack Mount. This kit contains mounting brackets, chassis track slides, mounting ears and a chassis track slide with a full 90° tilt capability.

1-9 ADDITIONAL EQUIPMENT REQUIRED

Either of the two pieces of equipment shown in Figure 1-4 below is required for normal 56100A operation.

SWR Autotester The 560 Series SWR Autotesters integrate in one small package a broadband, high directivity bridge, a detector, a low reflection test port, a reference termination, and a connecting cable. The output of the SWR Autotester is a detected signal, varying in proportion to reflections from the test device connected to the test port. Optional extender cables can be used without degradation in performance.

Detectors The 560 Series detectors are used for coaxial transmission loss or gain and power measurements and also with coaxial adapters for waveguide reflectometer measurements. Zero-biased, field-replaceable Schottky diodes provide –60 dBm sensitivity. Optional extender cables can be used without degradation in performance.

Figure 1-4. *560 Series SWR Autotester and Detector*

1-10 AVAILABLE ACCESSORIES

The accessories listed below and shown in Figure 1-5, are available for the 56100A.

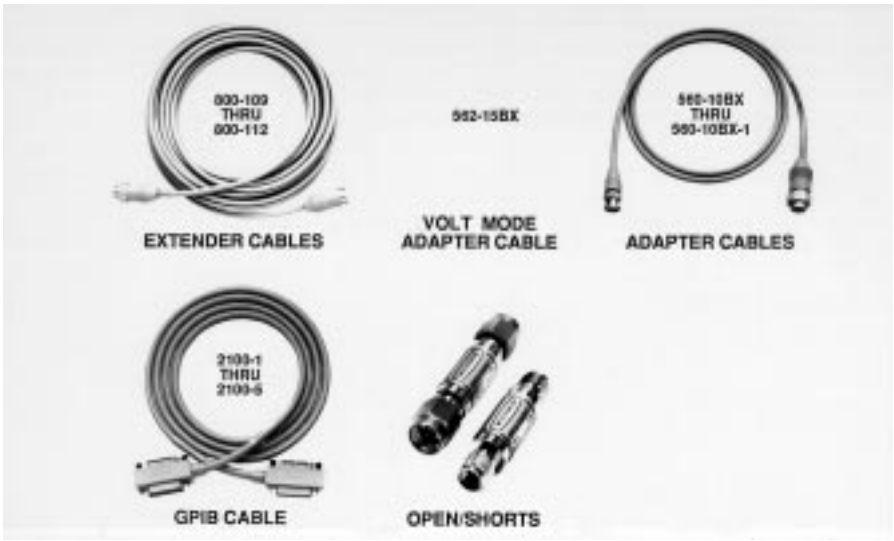


Figure 1-5. *Available Accessories for the 56100A*

Extender Cables Extender cables can be installed between the SWR Autotester or detectors and the 56100A, permitting measurements up to 200 feet. The available lengths are:

- 7.6m (25 ft.), P/N 800-109
- 15.2m (50 ft.), P/N 800-110
- 30.5m (100 ft.), P/N 800-111
- 61m (200 ft.), P/N 800-112

GPIB Cables The 2100- series cables interconnect instruments on the GPIB; the 2100-1 cable is provided with the 56100A. The available cable lengths are:

- 1m (3.3 ft.), P/N 2100-1
- 2m (6.6 ft.), P/N 2100-2
- 4m (13.2 ft.), P/N 2100-4
- 0.5m (1.65 ft.), P/N 2100-5

Adapter Cables

The 560- series adapter cables with BNC and SMA female connectors allow the 56100A to be used with waveguide or other detectors with the same type of output connectors. Cable length is 122 cm (4 ft.):

- BNC Female, P/N 560-10BX
- SMA Female, P/N 560-10BX-1

The 806- series of adapter cables are used to connect the 56100A to various sweep generators. The 806-7 cable is provided with the 56100A and is used to connect to ANRITSU 6600B and 6700A/B signal sources. Other cables available are:

- ANRITSU 56100A to HP 8350B, HP 8340A/B: P/N 806-13
- ANRITSU 56100A to HP 8620C: P/N 806-14

Open/Short Calibration References

An Open/Short is used to establish a 0 dB return loss reference during the normalization procedure for the 56100A. The available calibration references are:

- GPC-7 Short Only
- GPC-7
- K Male
- K Female
- N Male
- N Female
- WSMA Male
- WSMA Female

Other Accessories

Other accessories for the 56100A include:

- A transit case for the RF components
- A transit case for the instrument itself
- A 260 mm (10.25 in.) diagonal external monitor
- A Cannon BJ30 Ink Jet Printer

1-11 PERFORMANCE SPECIFICATIONS

Performance specifications for the 56100A are listed in the Technical Data Sheet located in Appendix A of the 56100A Operating Manual. They are also included as part of the procedures contained in Chapter 2 of this manual.

1-12 EXCHANGE ASSEMBLY PROGRAM

ANRITSU maintains a module exchange program for selected subassemblies. If a malfunction occurs in one of these subassemblies, the defective item can be exchanged. Upon receiving your request, ANRITSU will ship the exchange subassembly to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local ANRITSU Sales Company or ANRITSU Customer Service:

ANRITSU Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

ANRITSU Tables 1-1 and 1-2 provide a listing of replaceable subassemblies for the 56100A.

1-13 STATIC SENSITIVE COMPONENT HANDLING PRECAUTIONS

The 56100A contains components that can be damaged by static electricity. Figure 1-6 (page 1-15) illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

NOTE

Use of a grounded wrist strap when removing and/or re-placing subassemblies or parts is strongly recommended.

1-14 RECOMMENDED TEST EQUIPMENT

Table 1-3 page (1-16) provides a list of recommended test equipment needed to check and service the 56100A Scalar Network Analyzer.

Table 1-1. *Replaceable Subassemblies Listing*

Replaceable Subassembly	ANRITSU Part Number
A1/A2 Signal Channel PCB Assy	D42005-3
A2 Front Panel Interface PCB Assy	D40036-7
A3 Signal Channel Interface PCB Assy	D42003-3
A4 Sweeper Interface PCB Assy	D32659-3
A5 Input Connector PCB Assy	C42002-3
A7 CPU PCB Assy	D42001-3
A8 Graphics System Processor PCB Assy	D42004-3
A9 Motherboard PCB Assy	D42000-3
A12 Power Supply Assy	D32521-3
Monitor Assy	D40047
Front Panel Assy	B42055
Rear Panel Assy	B42056
Cable Assy, Main Power Switch	C42033
Power Supply Line Transformer	D32572

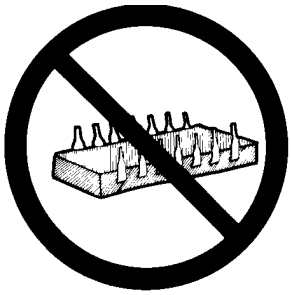
Table 1-2. *Replaceable Parts Listing (1 of 2)*

Description	Part Number
Cover, Top	D40107
Cover, Bottom	D40107
Cover, Side (Handle)	2000-633
Cover, Side	D42021
Handle, Side Carrying	783-830
Screw, Handle, Side Carrying	900-714
Connector, Front Panel Input	551-152
Foot, Rear, Bottom Left	2000-548
Foot, Rear, Bottom Right	2000-549
Foot, Rear, Top Left	2000-552
Foot, Rear, Top Right	2000-553
Screw, Green Head	2000-560
Fuse, 2A, Antisurge, 3AG (110/120 Vac Operation)	631-62
Fuse, 1A, Antisurge, 5x20 mm (220/240 Vac Operation)	631-63
Fuse Holder, 3AG	553-221
Fuse Holder, 5 x 20 mm	553-240
Fan Assembly, Rear Panel	C40217
Finger Guard, Fan (with filter, aluminum)	790-442
Knob, Data Entry	2000-641
Line Module Assembly, Rear Panel	260-13

Table 1-2. *Replaceable Parts Listing (2 of 2)*

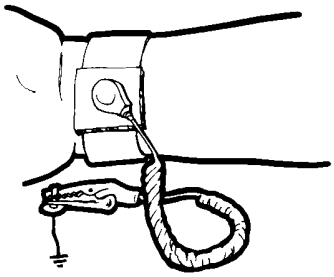
Description	Part Number
56100A Models Without Front Handles	
Foot, Front, Bottom Right	2000-546
Foot, Front, Bottom Left	2000-547
Foot, Front,Top Left	2000-550
Foot, Front,Top Right	2000-551
56100A Models With Front Handles	
Upper Insert	B37147
Foot, Bottom Left	C37170
Foot, Bottom Right	C37171
Handle, Left	D37168-3
Handle, Right	D37169-3

1. Do not touch exposed contacts on any static sensitive component.



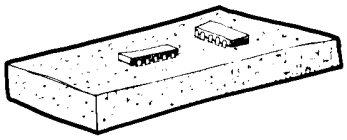
2. Do not slide static sensitive component across any surface.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

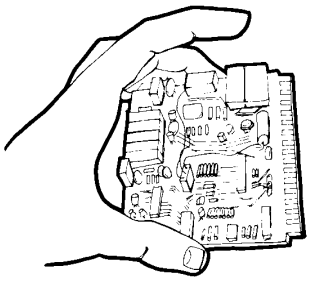


4. Wear a static-discharge wristband when working with static sensitive components.

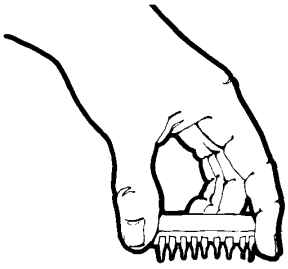
5. Label all static sensitive devices.



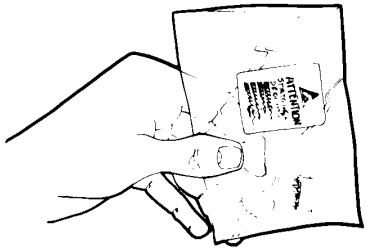
6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.



9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-6. *Static Sensitive Component Handling Procedures*

Table 1-3. *Recommended Test Equipment*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE*
Adaptor Cable	Simulates 560-7 Series detectors	ANRITSU Model 560-10BX	C, P
Adapters (50Ω impedance)	Type N (male) to BNC (male) Type N (female) to BNC (male)	HP1250-0176 HP1250-0082	C, P
Connector Cable	Connects sweep generator signal for 56100A compatibility	ANRITSU 806-7	C, P, O
GPIB Cable	Connects 56100A to 68147B via dedicated bus	ANRITSU 2100-1	C, P, O
RF Detector	0.01 to 20 GHz	ANRITSU Model 560-7N50B	C, P, O
Digital Multimeter	Resolution: 4-1/2 digits (to 20V) *DC Accuracy:* 0.002% + 2 counts *DC Input Impedance:* 10 MΩ *AC Accuracy:* 0.07% + 100 counts (to 20 kHz)	John Fluke Mfg Co. Inc., Model 8840A	C
Oscilloscope	*Bandwidth*: DC to 150 MHz *Sensitivity:* 2 mV *Horiz. Sensitivity:* 50 ns/division	Tektronix, Inc. Model 2445	C, P
Power Meter, with: Power Sensor 50Ω input	*Power Range:* +10 to –55 dBm *Other:* 50 MHz Calibrated Output Frequency Range: 1.0 MHz to 2.0 GHz *Power Range:* –30 to +20 dBm	Anritsu Corp., Model ML4803A Anritsu Corp., Model MA4601A	C, P
Frequency Source	*Frequency Range:* 0.01 to 20 GHz *Power Range: +10 dB to –60 dBm*	ANRITSU Model 681XXB Series ANRITSU Model 683XXB Series	C, P, O
Step Attenuator	*Attenuation Range:* 60 dB, 10 dB/step 0.000 to 18.0 GHz	Hewlett-Packard, Model 8495B	C, P
Voltage Standard	Range: –1.462V to –1.313 mV Accuracy: 0.002% of set value.	John Fluke Mfg Co. Inc., Model 335D	C, P

* C = Calibration, P = Performance verification, O = Operational

Chapter 2
Performance Verification

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Chapter 2
Performance Verification

2-1 INTRODUCTION

This section provides two procedures for verifying signal channel accuracy, the only test necessary to ensure that the 56100A provides proper performance. These two procedures provide alternative methods for checking signal channel accuracy.

2-2 RECOMMENDED TEST EQUIPMENT

Table 1-1 (Chapter 1) provides a listing of recommended test equipment for both the DC and RF methods. If the recommended items are not available, equipment with equivalent characteristics may be substituted.

2-3 VERIFYING SIGNAL CHANNEL ACCURACY

Two methods for verifying signal channel accuracy are described in this section. The first and most accurate is the DC Voltage Method, which uses highly accurate dc voltages applied directly to the signal channel being verified. Using this method, measurement uncertainties are negligible (provided that the recommended test equipment is used.) The second method is the RF Method that has measurement uncertainties attributable to the source, attenuator, and detector.

2-4 DC VOLTAGE METHOD

The dc voltage method uses highly accurate dc voltages to simulate input RF power without introducing source errors. A 560-10BX adapter cable must be used to connect the dc voltage to the input of the 56100A.

Step 1. Set up the test equipment as shown in Figure 2-1.

Step 2. Connect the 560-10BX cable to input A on the 56100A.

Step 3. Press the Power keys on the 56100A and 68147B to On.

Step 4. On the 56100A:

- Press the System Menu key.
- Using the Menu up/down keys, highlight **RESET (TO FACTORY SETTINGS)** and press the Select key (this resets both the 56100A and 68147B).
- Press the Channel 2 Display On/Off Key to Off.
- Ensure that INTERFACE OFF is not displayed on the bottom line and that frequencies are annotated correctly.
- Press the Channel 1 Menu key.
- Using the Menu up/down keys, highlight **POWER**.
- Press the Select key.

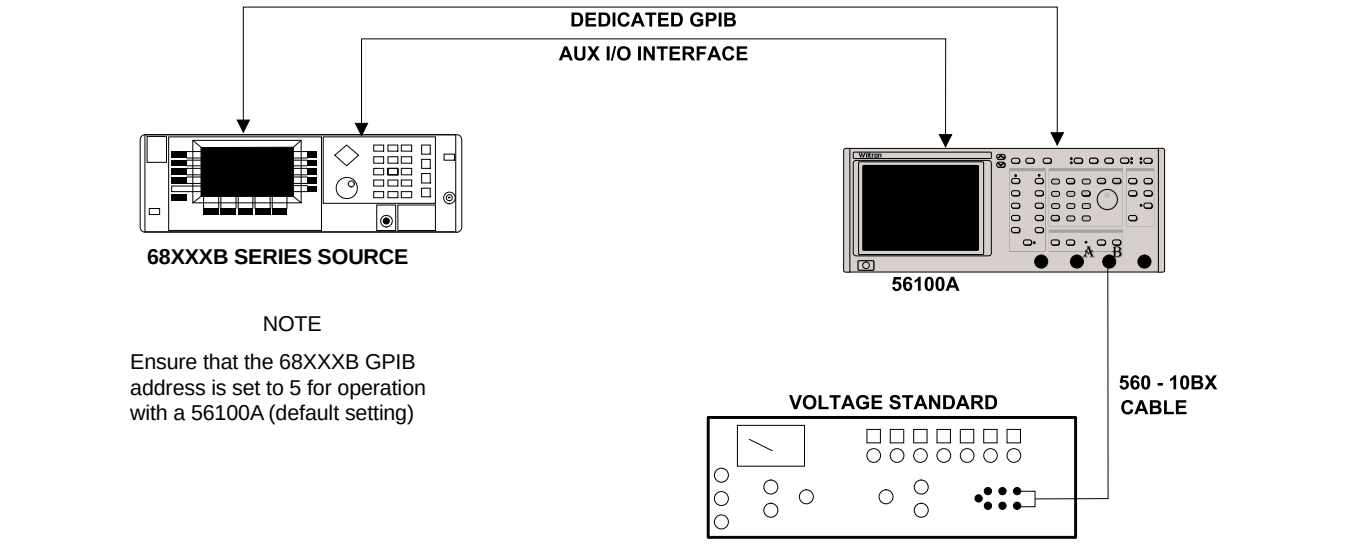

Figure 2-1. *Test Equipment Setup, DC Voltage Method*

- Press the Cursor Measurements On/Off key to On.

Step 5. On the 68147B:

- Go to the Configure RF Menu and press the Retrace RF key to On.

Step 6. Set the DC voltage source to zero volts. Press the Calibration key and select **LOW LVL TRIM** from the displayed menu.

Number	DC Voltage	CURSOR dBm Reading
1	–1.462V	+16, +0.25; –0.10
2	–0.6208V	+9, +0.12; –0.10
3	–1.313 mV	–26, ±0.34

Step 7. Adjust the voltage standard to provide voltage 1 in table at left.

Step 8. On the 56100A, verify that the CURSOR dBm value displayed in the menu area is within the tolerances listed in the table at left.

Step 9. Increment the voltage standard output to voltages 2 and 3, in turn, and repeat steps 7 and 8 (above). For voltage 3, press the Smoothing key to light both LEDs (maximum smoothing).

Step 10. Move the 560-10BX cable to input B.

Step 11. On the 56100A:

- Press the Channel 1 Menu key.
- Using the Menu up/down keys, highlight **SELECT INPUT** from the displayed menu.
- Press the Select key.
- Using the Menu up/down keys, highlight B.
- Press the Select key.
- Press the Cursor Measurements On/Off key to restart the numerical display in the menu area.
- Repeat steps 6 thru 9 for input B.
- Repeat steps 9 and 10 for R1 and R2. In the procedure, substitute “R1” and “R2,” respectively, for “B”.

2-5 RF TEST METHOD

The RF method for verifying signal channel accuracy has inherent measurement inaccuracies. These inaccuracies are explained in paragraph 2-6. Tables 2-1 and 2-2 list the expected accuracy limits and error sources introduced by the test equipment during these measurements. Table 2-1 has space where the Cursor dBm Readings may be recorded for these measurements.

Power Meter/Power Sensor Calibration at 50 MHz

Step 1. Position the CAL FACTOR control on the power meter to the necessary calibration power factor as specified on the power sensor chart.

Step 2. Zero set the power meter.

Step 3. Connect the power sensor to the POWER REF connector. With the POWER REF ON, adjust the CAL ADJ potentiometer for 0.00 dBm on the power meter display.

Step 4. Disconnect the power sensor from the POWER REF connector.

Sweep Generator/Step Attenuator Output Power Calibration

Step 1. Set up the test equipment as shown in Figure 2-2.

Step 2. Press the Power keys on the 56100A and 68147B to On.

Step 3. On the 56100A:

- Press the System Menu key.

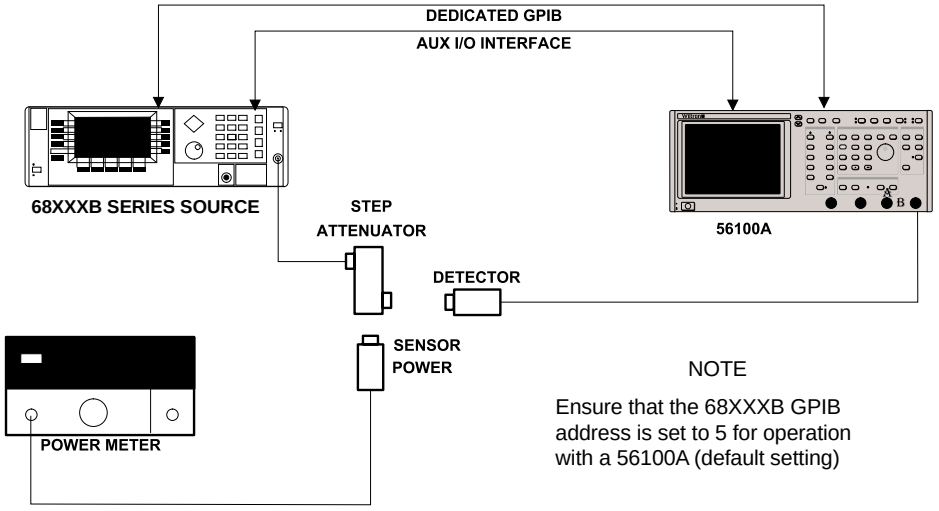

Figure 2-2. *Test Equipment Setup, RF Method*

Table 2-1. *Power Accuracy with Recommended Test Equipment*

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	RSS Limits (dBm)
0	10		10.6 to 9.5
10	0		0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9

Table 2-2. *Effect of Possible Error Sources on Measurement (RF Method)*

Input Powr (dBm)	Possible Error (dB) at 50 MHz					RSS Error
	Det/Source Match Interaction	Harmonic Frequency at 30 dBc	Attenuator Accuracy	Detector Frequency Response	Signal Channel Accuracy	
+16	±0.31	+0.6 –0.4	±0.3	+0.3 –0.2	+0.25 –0.1	+0.8 –0.7
+10	±0.28	+0.3 –0.2	±0.3	+0.3 –0.2	+0.15 –0.1	+0.6 –0.5
0	±0.14	+0.3 –0.2	±0.3	+0.3 –0.2	±0.2	+0.6 –0.5
–10	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.25	+0.6 –0.5
–20	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.3	+0.6 –0.5
–30	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.4	+0.7 –0.6
–40	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.5	±0.7
–50	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.8	+1.0 –0.9
–55	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±1.0	±1.1

- Using the Menu up/down keys, highlight **RESET (TO FACTORY SETTINGS).**
- Press the Select key (this resets both the 56100A and 68147B).

Step 4. On the 68147B, go to the Configure RF Menu and press the Retrace RF key to On.

Step 5. On the 355D:

- Position the attenuator dial to 10.
- Connect the power sensor to the output.

Step 6. On the 68147B:

- Press the CW/Sweep Select key to go to the CW Menu display.
- Press the Edit F1 key, and set F1 for 50 MHz.
- Press Edit F1 and set the output power for +5 dBm (nominal) using the keypad.
- Using the rotary data knob, adjust the output power to indicate –5 dBm on the power meter display.
- Record the indicated output power level from the 68147B Level display.
- Set the level to +10 dBm (nominal) using the keypad.
- Using the rotary data knob, adjust the output power to indicate 0.00 dBm on the power meter display.
- Record the indicated output power level from the Level display.

Channel A Power Accuracy Test

Step 1. On the 355D:

- Remove the power sensor.
- Connect the detector.
- Set the dial to 0.

Step 2. On the 68147B, go to the Configure RF Menu and press the Retrace RF key to Off.

Step 3. On the 56100A:

- Press the Channel 2 Display On/Off key to Off
- Press the Channel 1 Menu key.
- Using the Menu up/down keys, highlight **POWER**.
- Press the Select key.
- Press the Cursor Measurements On/Off key to On.

Step 4. Press the System Menu key and select data points. Set the data points to 101.

Step 5. Tabulate results as follows: Record the CURSOR readout from the display into Table 2-2, on the line for the corresponding Attenuator Dial Setting.

Step 6. On the 355D and 56100A, tabulate as in step 4, above, for settings of 10, 20, 30, and 40.

NOTE

Smoothing should be off throughout these tests.

Step 7. Position the 355D to 50.

Step 8. On the 56100A:

- Press the Averaging key.
- Use the Menu up/down keys to highlight 32 averages and Select.

Step 9. Tabulate the results as described in step 4, above.

Step 10. Position the 355D to 60.

Step 11. On the 56100A:

- Press the Averaging key. Use the up/down keys to highlight 128 sweeps and press select.

Step 12. Tabulate as described in step 1, above. The readout corresponds to a –50 dBm input power level.

Step 13. On the 68147B:

- Press the Edit F1 key, and using the keypad enter the level as recorded during "Sweep Generator/Step Attenuator Output Power Calibration" in step 6 (5th bullet) on page 2-8.
- Averaging starts automatically when the 68147B changes level.
- Tabulate as described in step 4, above. The readout corresponds to –55 dBm input power level.

Channel B Power Accuracy Test

Step 1. On the 56100A:

- Press the Averaging key twice to turn averaging off.
- Press the Channel 1 Menu key.
- Using the Menu up/down keys, highlight **SELECT INPUT**.
- Press the Select key.
- Using the Menu up/down keys, highlight B.
- Press the Select key.
- Move the detector to the B input.
- Press the Cursor Measurements On/Off key to On to restore the numerical display in the menu area.

Step 2. On the 68147B:

- Press the Edit F1 key.
- Using the keypad and appropriate terminator key, set the output power for the value recorded in Step 6 (last bullet) on page 2-8.

Step 3. On the 355D, position the attenuator dial to 0.

Step 4. Go to page 2-8 and repeat Steps 2 thru 13 as listed for the Channel A Power Accuracy Test.

Channels R1 and R2 Power Accuracy Tests

Repeat the procedure or the Channel A Power Accuracy Test for inputs R1 and R2. Substitute “R1” and “R2,” respectively, for “A.”

2-6 INHERENT UNCERTAINTIES IN RF TEST METHOD

The power measurement method using the recommended test equipment listed in Table 1-1 (Chapter 1) and shown in Figure 2-2 contains inherent measurement uncertainties. These uncertainties are explained in the following paragraphs.

Detector/Source Match Interaction Uncertainty

The impedance mismatch between the RF source and the RF detector contributes a possible uncertainty known as source match. For the 68147B and the 560-7 Series detectors, this uncertainty is as follows:

At +10 dBm (355D Attenuator Dial at 0), the source match of the sweep generator and the mismatch of the RF detector interact to produce an overall uncertainty of ±0.28 dB.

At 0 dBm and below (355D Attenuator Dial between 10 and 60), the source match of the 355D and the RF detector interact to produce an uncertainty of ±0.14 dB.

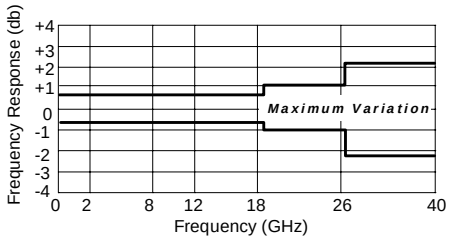

Figure 2-3. *Detector Frequency Response*

Sweep Generator Harmonics

In the linear range of the RF detector (between +16 dBm and approximately –15 dBm) harmonics of the sweep generator fundamental frequency contribute to errors in the measurement.

Step Attenuator Accuracy

The HP355D step attenuator has a specified accuracy of ±0.3 dB from dc to approximately 50 MHz. This possible error in accuracy is present at all attenuator dial settings, including zero.

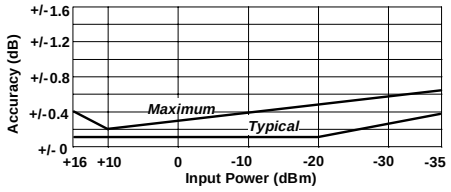

Figure 2-4. *Channel Accuracy*

Detector Frequency Response

The frequency response of the Model 560-7 detector introduces a further possible error as shown in Figure 2-3.

Signal Channel Accuracy

The accuracy varies with input power as shown in Figure 2-4. Be advised that the values used in Table 2-4 are factory test values. They are much tighter than the published accuracy as shown in Figures 2-3 and 2-4.

2-7 PERFORMANCE TEST RECORD

Copies of sample performance test records are provided below in Tables 2-3 and 2-4. These test records provide the means for maintaining an accurate and complete record of instrument performance. We recommend that you copy these pages and record on them the results from your initial testing of the 56100A. These initial readings can later be used as benchmark values for future tests of the same serial-numbered instrument.

DC Voltage Method Verification Test

Table 2-3 below provides a place for recording the values measured for Inputs A, B, R1 and R2 during the DC Voltage Method channel verification test.

Table 2-3. *Sample Test Record for DC Voltage Method Verification Test*

Input A, Channel 1

Number	DC Voltage	CURSOR dBm Reading (Spec)	CURSOR dBm Reading Rec'd
1	–1.462V	+16, +0.25; –0.10	
2	–0.6208V	+9, +0.12; –0.10	
3	–1.313 mV	–26, ±0.34	

Input B, Channel 1

Number	DC Voltage	CURSOR dBm Reading (Spec)	CURSOR dBm Reading Rec'd
1	–1.462V	+16, +0.25; –0.10	
2	–0.6208V	+9, +0.12; –0.10	
3	–1.313 mV	–26, ±0.34	

Input R1, Channel 1

Number	DC Voltage	CURSOR dBm Reading (Spec)	CURSOR dBm Reading Rec'd
1	–1.462V	+16, +0.25; –0.10	
2	–0.6208V	+9, +0.12; –0.10	
3	–1.313 mV	–26, ±0.34	

Input R2, Channel 1

Number	DC Voltage	CURSOR dBm Reading (Spec)	CURSOR dBm Reading Rec'd
1	–1.462V	+16, +0.25; –0.10	
2	–0.6208V	+9, +0.12; –0.10	
3	–1.313 mV	–26, ±0.34	

RF Method Verification Test

Table 2-4 below provides a place for recording the values measured for Inputs A, B, R1 and R2 during the RF Method channel verification test. We recommend that you copy these pages and record on them the results from your initial testing of the 56100A.

Table 2-4. *Sample Test Record for RF Method Verification Test*

Input A, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	10		10.6 to 9.5
10	0		0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

Input B, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	10		10.6 to 9.5
10	0		0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

Input R1, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	10		10.6 to 9.5
10	0		0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

Table 2-4. *Sample Test Record for RF Method Verification Test (Cont.)*

Input R2, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	10		10.6 to 9.5
10	0		0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

Chapter 3
Adjustments

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Chapter 3
Adjustments

3-1 INTRODUCTION

This chapter contains the adjustment procedures for the Model 56100A. A performance verification test, using the DC Voltage Method, is also included at the end of paragraph 3-3. These procedures are usually used when out-of-specification conditions are noted during the Performance Verification tests of Chapter 2, or as a result of subassembly/component repair or replacement.

3-2 RECOMMENDED TEST EQUIPMENT

Table 1-1 (Chapter 1) lists the recommended test equipment for performing the adjustment procedures contained in this section.

3-3 ADJUSTMENT PROCEDURES

To perform the adjustment procedures, the top cover and the PCB card clamp must be removed.

Step 1. Set up the test equipment as shown in Figure 3-1.

Step 2. With the 56100A off, press the Power key on the 68147B and allow the self test to finish.

Step 3. Press the Reset key on the 68147B.

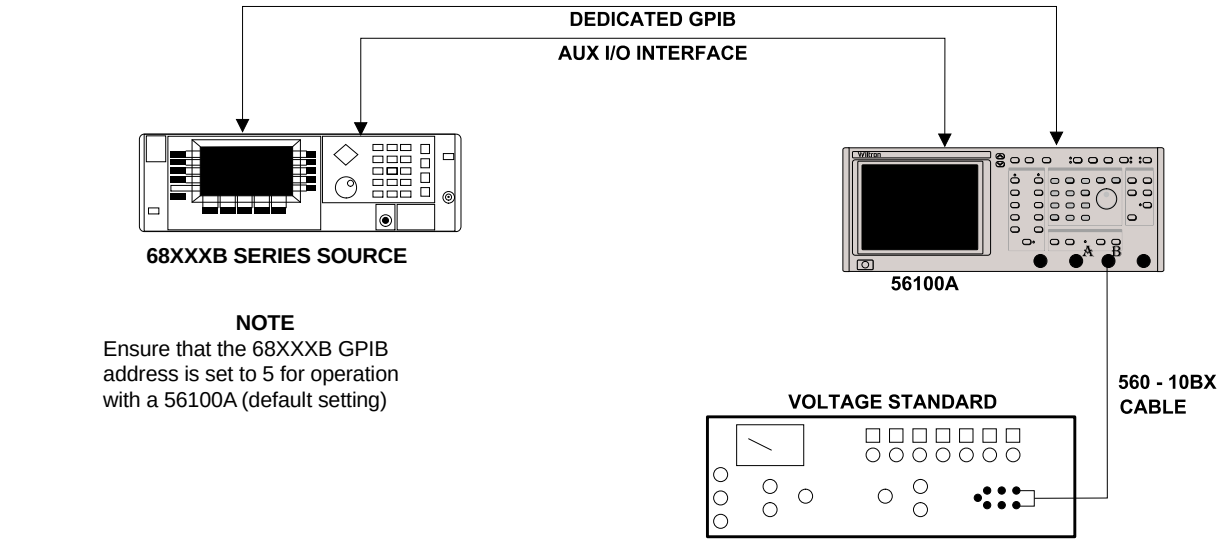

Figure 3-1. *Test Equipment Setup, DC Voltage Method*

Step 4. Press the 56100A Power key and allow the self test to finish.

NOTE

Unless otherwise specified, the 56100A is the instrument referred to in the following steps.

Step 5. Press the System Menu key.

Step 6. Use the Menu up/down keys to highlight **RESET**.

Step 7. Press the Select key.

Step 8. Press the Channel 2 Display On/Off key to turn off the corresponding LED.

Step 9. Press the Channel 1 Menu key.

Step 10. Use the Menu up/down keys to highlight **POWER.**

Step 11. Press the Calibration key.

Step 12. Repeatedly press Down cursor key until Log/Temp correction is highlighted.

Step 13. Press the Select key.

CAUTION

Be careful not to disturb the front panel keys when making the following A1/A2 PCB adjustments.

Step 14. Connect the 560-10BX cable to the A input. Leave the BNC end of the cable disconnected.

Step 15. Adjust A2R62 for 0.00 ±0.01, as read on the LOG/TEMP CORRECTION display (see Figure 3-2).

Step 16. Remove the cable from the A input and connect it to the B input.

Step 17. Adjust A2R64 for 0.00 ±0.01.

Step 18. Remove the cable and connect it to the R1 input.

Step 19. Adjust A1R62 for 0.00 ±0.01.

Step 20. Remove the cable and connect it to the R2 input.

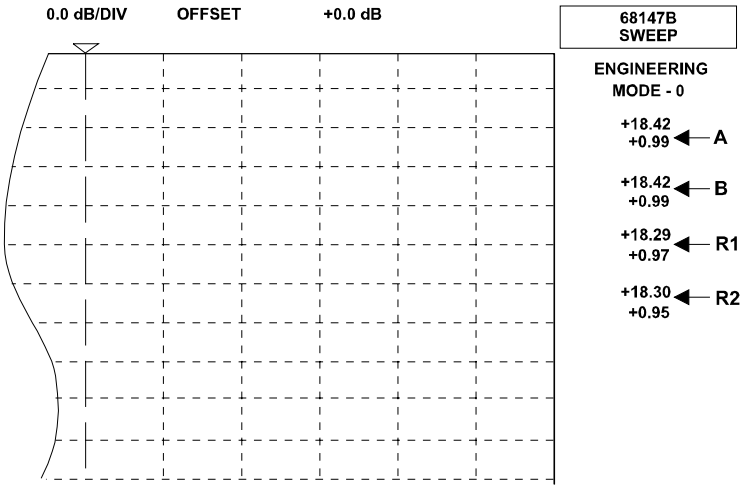

Figure 3-2. *Monitor Display of LOG/TEMP CORRECTION*

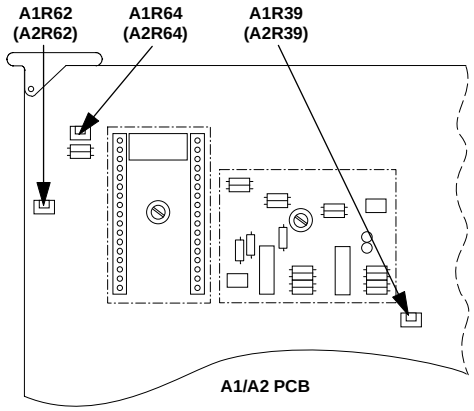

Figure 3-3. *A1/A2 PCB Adjustments*

Step 21. Adjust A1R64 for 0.00 ±0.01.

Step 22. Press the Cursor Measurements On/Off key to On. A cursor display should appear on the upper right side of the monitor screen.

Step 23. Set the voltage standard for a –0.6208V output, which is equivalent to +9 dBm.

Step 24. Connect the cable to the A input.

Step 25. Connect the BNC end of the cable to the voltage standard.

Step 26. Adjust A2R39 until the cursor readout is +9 dBm ±0.02 dB.

Step 27. Press the Channel 1 Menu key.

Step 28. Toggle the Menu up/down keys to highlight **SELECT INPUT.**

Step 29. Press the Select key.

Step 30. Use the Menu up/down keys to highlight **R1**.

Step 31. Press the Select key.

Step 32. Leaving the BNC end of the cable connected to the voltage standard, connect the other end to the R1 input.

Step 33. Press the Cursor Measurements On/Off key to Off to restore the cursor display.

Step 34. Adjust A1R39 until the cursor readout is +9 dBm ±0.02 dB.

NOTE

Steps 35 through 55 constitute a performance verification test utilizing the DC Voltage Method.

Step 35. Disconnect the BNC end of the cable from the voltage standard, and connect the other end to the A input.

Step 36. Press the Channel 1 Menu key.

Step 37. Toggle the Menu up/down keys to highlight **SELECT INPUT.**

Step 38. Press the Select key.

Step 39. Use the Menu up/down keys to highlight **A.**

Step 40. Press the Select key.

Step 41. Press the Calibration key.

Step 42. Using the Menu up/down keys, highlight **LOW LVL TRIM.**

Step 43. Press the Select key twice. Wait until the NULLING message disappears and a cursor display appears.

Step 44. Adjust the voltage standard to provide Voltage 1 in the table at left.

Step 45. Connect the BNC end of the cable to the voltage standard.

Number	DC Voltage	CURSOR dB Reading
1	–1.462V	+16, 0.25; 0.10
2	–0.6208V	9, 0.12; –0.10
3	–1.313 mV	–26, ±0.34

Step 46. Verify that the displayed CURSOR dBm value is within the tolerances listed in the above table.

Step 47. Increment the voltage standard output to voltages 2 and 3, in turn, and verify that the displayed CURSOR dBm value is within the tolerances listed in the table. When using voltage 3, set smoothing to minimum by pressing the Smoothing key to light the top LED.

Step 48. Disconnect the BNC end of the cable from the voltage standard, and connect the other end to input B.

Step 49. Press the Channel 1 Menu key.

Step 50. Using the Menu up/down keys, highlight **SELECT INPUT.**

Step 51. Press the Select key.

Step 52. Using the Menu up/down keys, highlight **B**.

Step 53. Press the Select key.

Step 54. Repeat steps 41 through 47 above.

Step 55. Repeat steps 48 through 54 for R1 and R2. In the procedure, substitute R1 and R2, respectively, for B.

3-4 SWEEP RAMP AMPLIFIER GAIN ADJUSTMENT

This procedure covers adjustment of the Sweeper Interface (A4) PCB Assembly, using a 56100A chassis and a 56100A PCB Extender card. This procedure is only required after repair or replacement of the A4 PCB.

Connect a function generator to an oscilloscope. On the function generator, select a triangular waveform and a frequency of 100 Hz. Set the amplitude to 13V peak to peak while monitoring the signal on the oscilloscope. Adjust the offset so that the upper limit of the signal is +12V and the lower limit is –1V.

Ensure that the 56100A is not in Ramp Output mode by using the Reset feature. Without altering any of its settings, disconnect the function generator from the oscilloscope and connect it to the BNC connector marked Horizontal Input/Output on the rear panel.

Attach a x10 probe to the oscilloscope. Connect the probe to TP2 and the ground clip to TP6 (0V).

The oscilloscope should show a triangular wave of 100 Hz at ≈10 $V_{p\text{-}p}$ amplitude. Adjust R10 until the upper limit of the waveform is exactly 10V above the 0V level. This completes the adjustment and verification of the Sweep Ramp circuit.

3-5 CRT MONITOR ADJUSTMENTS

These procedures are used to adjust the CRT monitor brightness, contrast, and horizontal size. Perform this procedure whenever a new CRT monitor assembly or Graphics Processor PCB has been installed. All other CRT monitor adjustments should be performed by qualified service personnel only.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. These procedures should only be performed by service personnel who are fully aware of the potential hazards associated with high voltage.

Required Equipment

☐ Adjustment of the CRT horizontal size requires the use of a plastic or nylon hex alignment tool. Do not use metal tools to adjust CRT monitor settings.

Preliminary

☐ Remove the 56100A top and left side covers, then set them back loosely in place.

NOTE

For this procedure, it is important that a consistent temperature be maintained within the unit. These adjustments must be made with the instrument at normal operating temperature.

Brightness and Contrast Adjustment

Step 1. Refer to the locator drawing on the CRT Monitor assembly top cover and locate the brightness and contrast trim pots, accessible through the side opening (Figure 3-4).

Step 2. Reset the instrument.

Step 3. Using the front panel INTENSITY control, set the display to intensity level 9.

Step 4. Carefully adjust the brightness and contrast trim pots until the display just starts to “bloom” or distort.

Step 5. Set the display intensity to level 1.

Step 6. Adjust, if required, the brightness and contrast to achieve a level that is just visible.

Step 7. Repeat steps 2 through 6 until the desired intensity levels at 1 and 9 are achieved.

Step 8. Replace the 56100A top and left side covers.

Step 9. Verify that the adjustment remains as desired throughout the operating temperature range of the instrument.

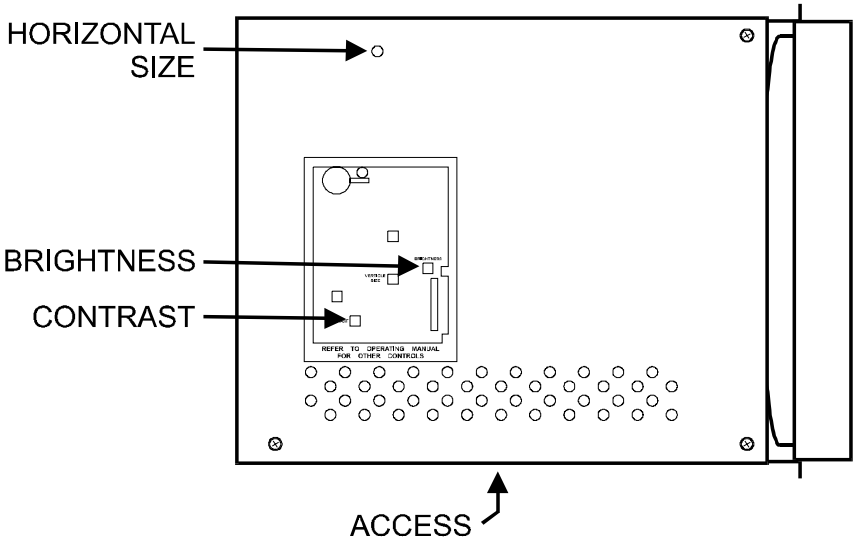

Figure 3-4. *CRT Monitor Adjustments*

Horizontal Size Adjustment

Step 10. Remove the 56100A top cover.

Step 11. Insert a plastic or nylon hex alignment tool through the access hole (see Figure 3-4) and carefully adjust the horizontal size coil until the display is centered on the CRT.

Step 12. Replace the 56100A top and side covers.

Step 13. Verify that the adjustment remains as desired throughout the operating temperature range of the instrument.

Chapter 4
Troubleshooting

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Chapter 4
Troubleshooting

4-1 INTRODUCTION

This chapter provides troubleshooting information for the 56100A Scalar Network Analyzer.

4-2 TROUBLESHOOTING PROCEDURES

Tables 4-1 and 4-2 list the Control Panel LED Error Codes for the 56100A. Figures 4-1 and 4-2 are the main troubleshooting chart. Table 4-2 contains notes for the troubleshooting chart. Figures 4-3 and 4-4 are auxiliary troubleshooting charts.

Table 4-1. *Control Panel LED Error Codes*

FLASHING LED*	FAULT	FAULT LOCATION
Top Averaging	Ramp Not Calibrated	A4, or Sweep Ramp Too Slow
Top Smoothing	CPU EPROM Checksum	A7 CPU (Observe Initial Test To Identify)
Bottom Averaging	CPU RAM Failure	A7 CPU
Bottom smoothing	Front Panel Keyboard Interface Failure	Front Panel
Hold	7210 GPIB Interface Failure	A7 CPU
Plotter	ADC Converter	A3 PCB
Remote	Channel R1/R2 PCB Not Detected	A1 (A3) PCB
Printer	Channel A/B PCB Not Detected	A2 (A3) PCB
Uncal	Channel R1/R2 PCB Null/Zero Failure	A1 (A3) PCB
Display CH1	Channel A/B PCB Null Zero Failure	A2 (A3) PCB

***** After a period of flashing, the option is given, at the user's discretion, to continue to attempt operation by pressing SELECT.

Table 4-2. *Memory Test LED Error Codes*

Flashing Led*	Fault	Fault Location
Hold and Plotter	Memory Test Result	N/A
Top Averaging	U36 RAM Failure	A7 CPU PCB
Bottom Averaging	U30 EPROM Checksum	A7 CPU PCB
Top Smoothing	U31 EPROM Checksum	A7 CPU PCB
Bottom Smoothing	U32 EPROM Checksum	A7 CPU PCB

56100A Control Panel LED Error Codes

When the 56100A is turned on, or when Self Test is selected, the analyzer undergoes a comprehensive self test. If this test passes, the message "ALL TESTS PASSED" is displayed; however, if any part of the self test fails, a descriptive error message is displayed. Additionally, a control panel LED flashes, indicating a fault condition exists. A different control panel LED flashes for each different type of fault condition. The control panel LED associated with each type of fault is listed in Table 4-1.

56100A Troubleshooting Charts

To use the troubleshooting charts for the Model 56100A: start at the top of the main troubleshooting chart (Figures 4-1 and 4-2) and proceed down the chart, performing the operations indicated. Refer to the auxiliary troubleshooting charts contained in Figure 4-3 and Figure 4-4 whenever so directed by the main troubleshooting chart. The notes for the main troubleshooting chart (Figures 4-1 and 4-2) are listed below in Table 4-2.

The suspected fault location will be indicated as a PCB or circuit location. If a replacement PCB is available, swap out the suspected PCB indicated by the chart. Otherwise, troubleshoot as applicable.

Table 4-3. *Notes for Troubleshooting Charts*

1. 56100A should start swept trace display, if connected to frequency source.
2. 56100A Text and Graphics processor should display short message indicating possible faults.
3. "Intellegent" sweepers only (ANRITSU 6600 series, or equivalent); all others ignore this step.
4. Sweep time of frequency source should be less than 2 seconds, maximum.
5. Verify cable connections and GPIB addresses for 56100A and for frequency source.
6. Frequency source firmware revision requirements:

6600A (with Memory Expansion)	7.22/7.05 or subsequent
6600B	8.07/6.05 or subsequent
6700A	6.13/3.0 or subsequent
6700B	7.04/4.01 or subsequent
HP 8350B	Refer to instrument manual.
HP 8341	Refer to instrument manual.

7. During initial portion of self test sequence, Hold and Plotter LEDs (only) should flash.
8. Any LED flashing simultaneously with the Hold and Plotter LEDs during self test indicates memory error.
9. If memory failure is not total, then self test failure message will identify probable failed IC.

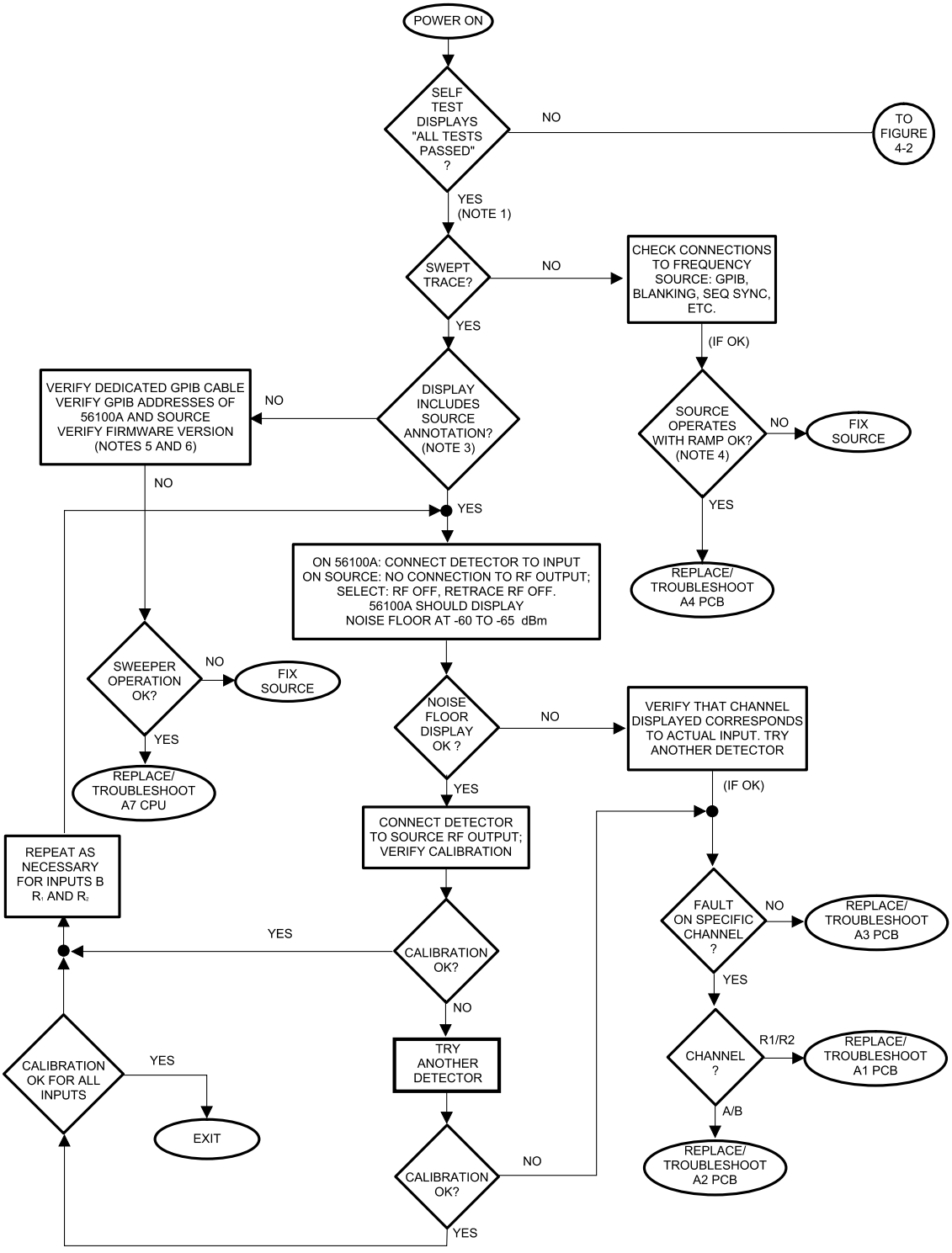

Figure 4-1. *Main Troubleshooting Chart*

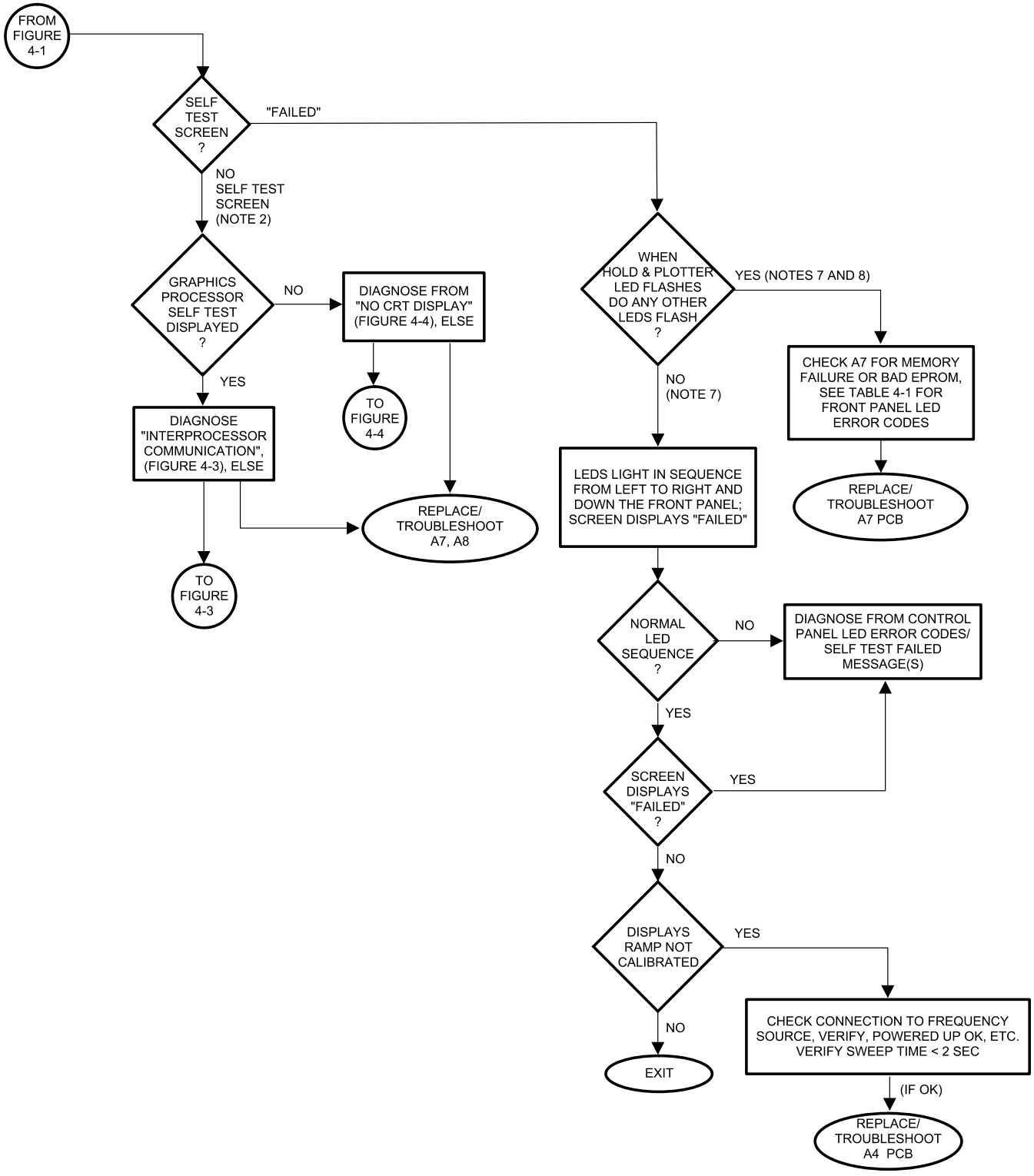

Figure 4-2. *Main Troubleshooting Chart*

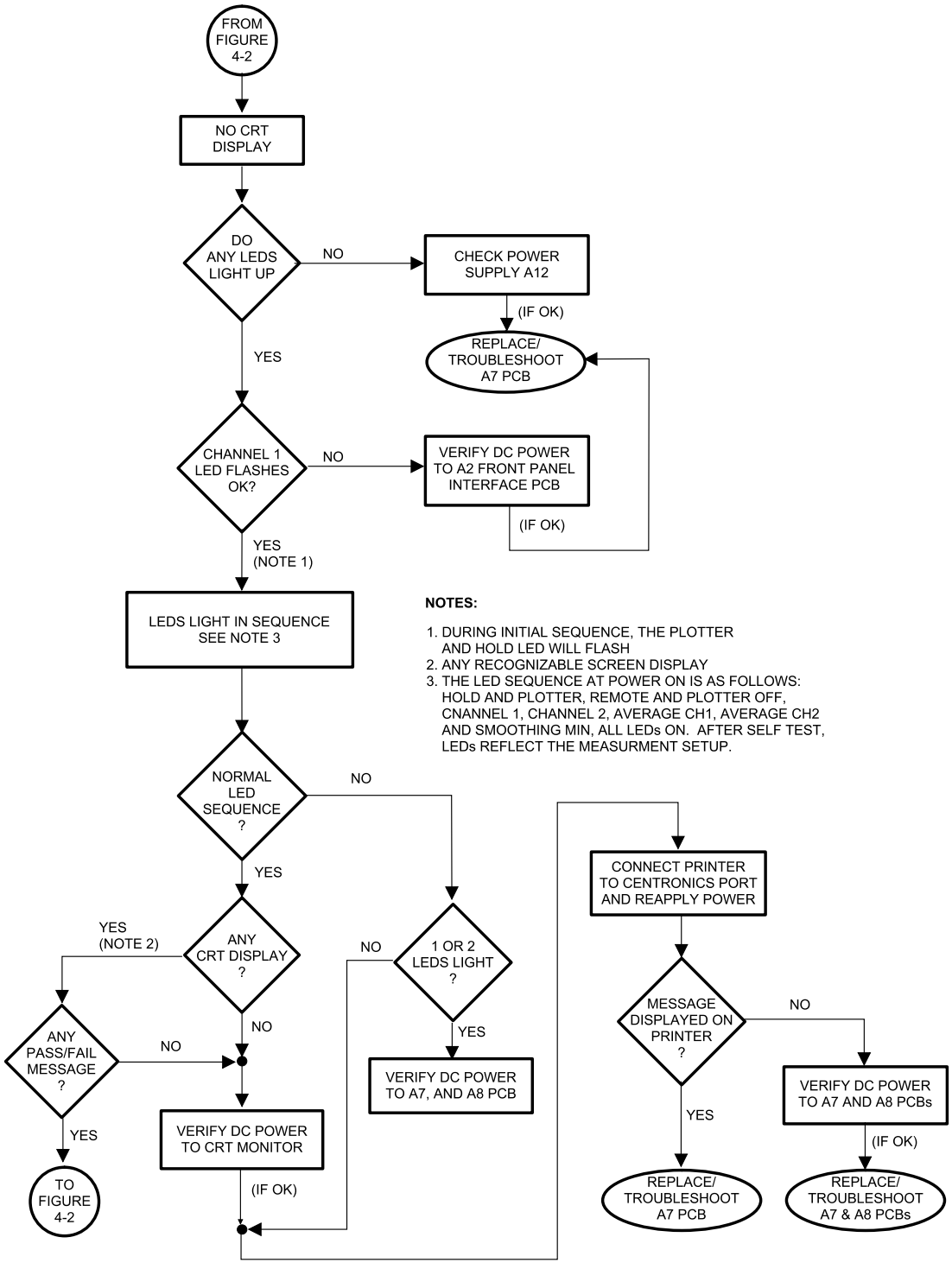

Figure 4-3. *Auxiliary Troubleshooting Chart 1*

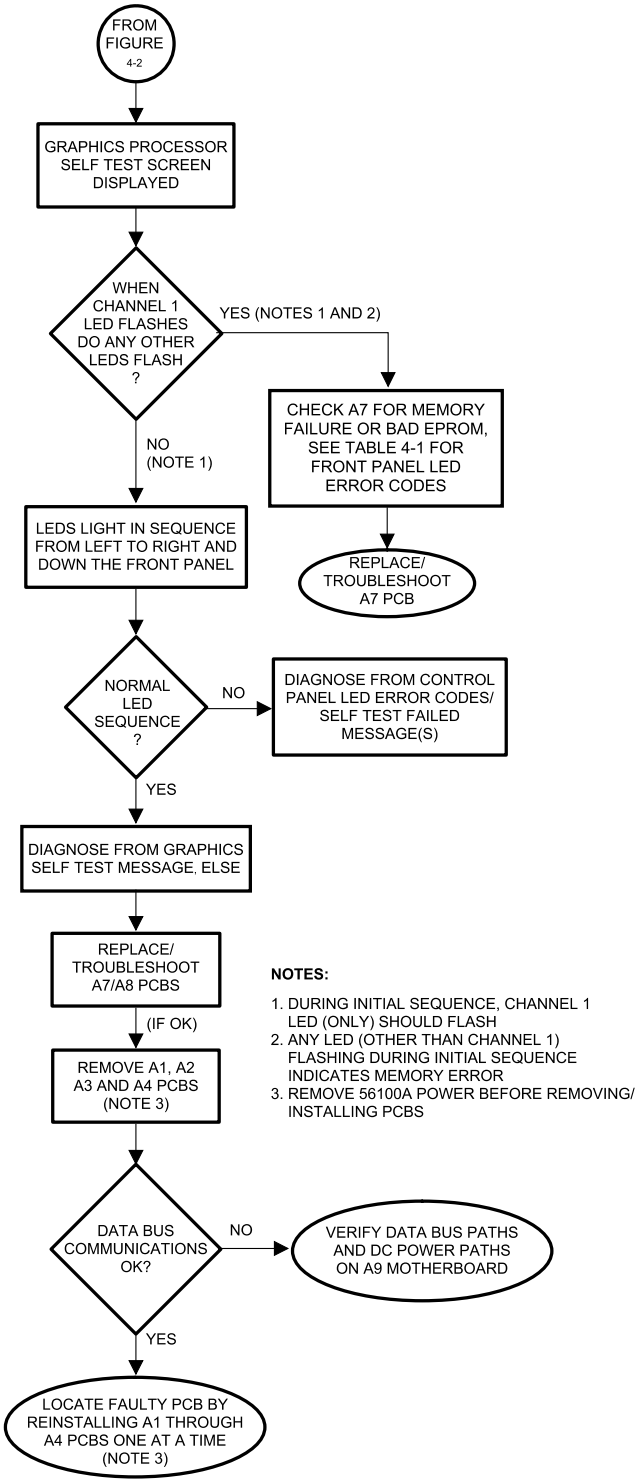

Figure 4-4. *Auxiliary Troubleshooting Chart 2*

Chapter 5
Functional Description

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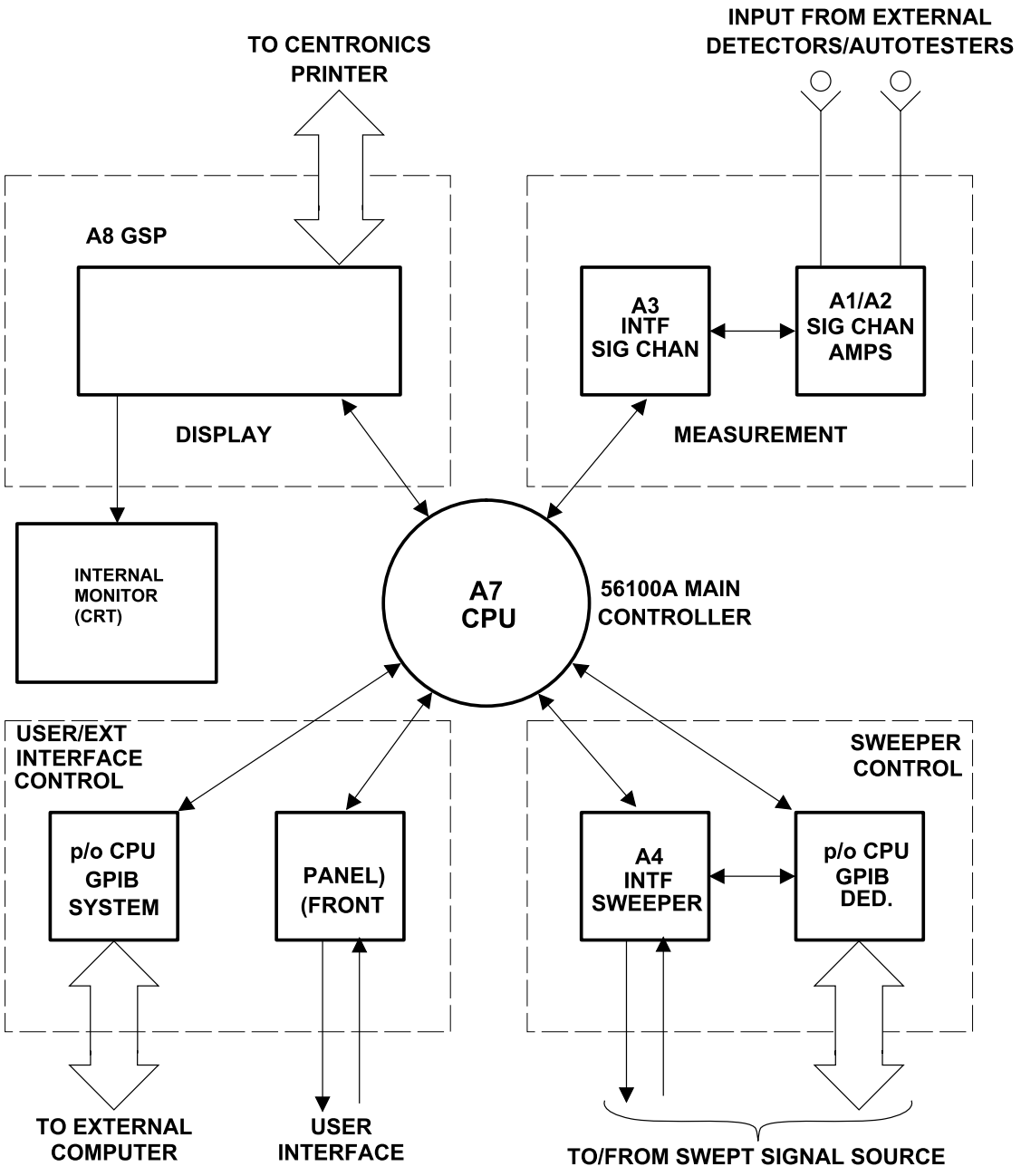

Figure 5-1. *Overall Block Diagram of Typical* ***56100****A Scalar Network Analyzer*

Chapter 5
Functional Description

5-1 INTRODUCTION

This chapter provides descriptions of the functional operation of the major assemblies contained in the 56100A Scalar Network Analyzer. The operation of each of the major circuit blocks is described. (The CRT monitor assembly is not covered in this chapter — this assembly is replaced as an entire unit.)

5-2 OVERVIEW OF 56100A OPERATION

The 56100A is a Scalar Network Analyzer (SNA) that uses state-of-the-art digital control and computational circuitry to enhance measurement accuracy and repeatability. An overall block diagram of the 56100A is shown in Figure 5-1 (facing page).

The central processing unit (CPU) of the 56100A is a 8088 microprocessor with a sixteen-bit internal bus and an eight-bit external bus. This microprocessor is located on the A7 PCB and communicates with all other subsystems through a main bus located on the motherboard. Functions that are monitored and controlled by the CPU include measurement (A1, A2, and A3), display (A8), printing (A8), sweeper interface (A4), plotting (A8), GPIB external control (A7), and the user interface (Front Panel A2). Figure 5-1 illustrates the interaction of these PCBs.

The interface to all of the PCBs listed above is memory mapped. This means that each function that the 56100A performs is at a specific address that the CPU either reads data from or writes data to. Each PCB may therefore have as many addresses mapped to it as are needed to communicate with the CPU.

The CPU is interrupt driven, meaning that when a particular subassembly must communicate with the CPU it generates an interrupt request (IRQ). The CPU then services each interrupt based on when it was generated and the level of priority assigned to that particular interrupt.

The Measurement Process

One of the major differences between the Model 56100A Scalar Network Analyzer and more conventional SNAs (such as the Model 560) is the use of linear amplifiers instead of log amplifiers. The data conversion to logarithmic form is performed digitally using look-up tables. This allows for more stable/accurate measurements and easier calibration than more conventional oscilloscope-like SNAs.

Printed circuit boards A1 and A2 are identical PCBs that process different channels of measurement data. The A1 PCB processes the R1 and R2 channels and the A2 PCB processes the A and B channels. Since these two PCBs are functionally identical, they are interchangeable. These units consist of an input (switching) module, switched-gain amplifiers, filters, a multiplexer, nulling circuits, a sample and hold amplifier, and log conformity and temperature compensation circuits.

The input module of each A1/A2 PCB uses switching field effect transistors (FETs) to multiplex the two input channels and provide a high impedance measurement input. Additional FETs break the signal path and provide a short circuit to the input of the amplifier chain for purposes of autozeroing.

Nulling circuitry for each measurement channel generates a feedback signal that is used to null out dc offsets produced by the amplification circuitry. These nulling signals are connected to the amplifier via the input module; the input module switching paths for these signals are controlled by the 56100A CPU.

The output signal from the input module goes to the input of the amplifier chain. The input circuit of the amplifier chain is comprised of a differential input instrumentation amplifier that provides high common mode rejection and a programmable gain of X1, X10, X100, and X1000. Two additional programmable gain stages provide an available overall gain of one million and boost the signal voltages to the levels required.

Filtering is achieved using switched capacitor filters to smooth the amplified signal. The desired level of smoothing is achieved by switching in different values of capacitors (or none).

Compensation for temperature variation is achieved via a thermistor contained in the external SWR Autotesters and/or detectors used with the 56100A. These thermistors are connected to voltage divider networks within the 56100A; the value of the resultant voltages are digitized and used by the CPU to produce measurement corrections. The log conformity correction is achieved in a similar manner via the log conformity resistors contained within the external test components.

The multiplexer switches the signal from the output of the amplification and filtering circuits as well as the temperature compensation and log conformity compensation voltages to the input of the sample and hold amplifier.

The sample and hold amplifier samples the output from the multiplexer and is the final stage of the A1/A2 Signal Channel Amplifier PCB. This circuit provides the input to the A3 Signal Channel Interface PCB.

The circuitry located on the A3 Signal Channel Interface PCB digitizes the signals from the A1/A2 PCBs. Other circuits on this board provide control signals for the A1/A2 PCBs and drive signals for the internal quiet data bus.

Sweeper Interface and Control

The A4 PCB contains the circuitry required to interface the 56100A to an external sweep generator/swept frequency synthesizer. This PCB uses the analog voltages provided by the swept signal source that were originally intended for conventional analog type SNAs. These analog voltages are converted to the necessary digital information required to interface to the 56100A CPU. Using this information, the A4 PCB generates a ramp output signal and dwell signals required by the swept signal source when generating signals at discrete frequency points. The ramp output signal from the A4 PCB may also be used externally for various test purposes, such as controlling voltage tuned oscillators (VTOs) or other devices.

Main CPU

The CPU circuitry for the 56100A is contained on the A7 PCB. It consists of a microprocessor, battery-backed nonvolatile RAM, decode logic for the I/O Ports and a ROM-based operating system.

The CPU controls the 56100A. As described above, it interfaces with all major subcircuits and monitors and controls these circuits. The operating system is ROM-based and contains the necessary instructions and data to control all of the primary functions of the 56100A. The Battery-backed RAM allows setup information to be retained, even when the 56100A is powered down and disconnected from line power.

The decode circuitry decodes the addresses of the RAM, ROM, and I/O ports used to interface with the

rest of the instrument. The I/O ports control the interface to the other subassemblies in the 56100A and with external equipment.

Screen Display and Hardcopy Output

The Graphics System Processor (GSP), is contained on the A8 PCB. This is a graphics subsystem that controls the monitor display and the printing capabilities of the 56100A. The CPU treats the GSP as an intelligent terminal and communicates with it through a combination of ASCII characters and escape sequences.

The hardcopy interface controlled by the A8 PCB consists of a 50k byte buffer and a Centronics compatible hardware driver circuit. This function is interrupt driven.

GPIB Functions

The A7 PCB is the interface to the 56100A system General Purpose Interface Bus (GPIB). It contains all the necessary control circuitry required for handshaking and data transfer via the system GPIB bus. The A7 PCB also contains the dedicated GPIB interface used to control an external swept signal source or a plotter.

Miscellaneous 56100A Functions

All 56100A PCBs plug into and/or are connected to the A9 Motherboard PCB. The motherboard contains all dc power distribution paths, signal paths, a main CPU bus, and a quiet data bus.

5-3 A7 CENTRAL PROCESSOR PCB

The A7 PCB is described below. A block diagram of these circuits is shown in Figure 5-2.

Central Processor Circuits The 56100A central processor is implemented using an Intel 8088 microprocessor. In addition to the microprocessor, the following circuits are used:

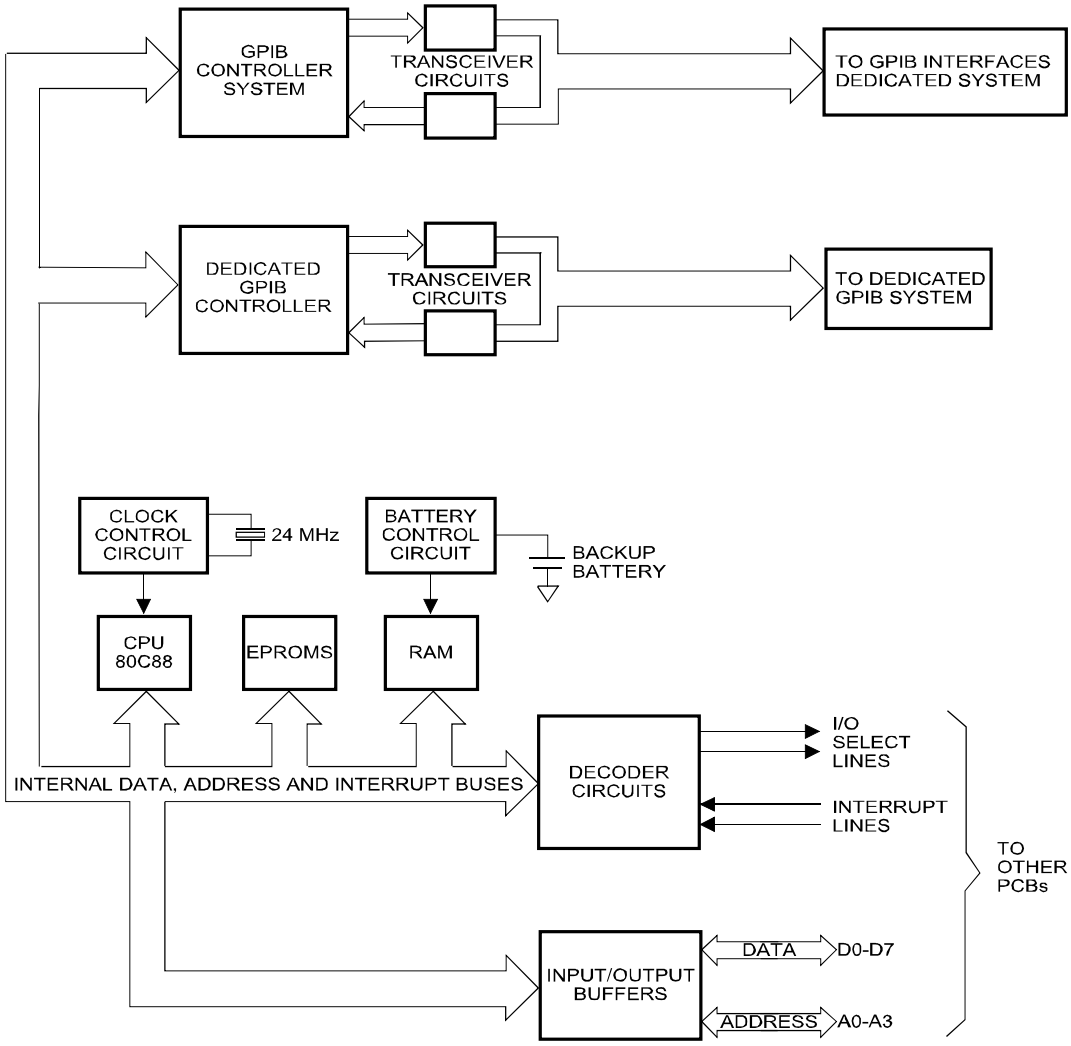

Figure 5-2. *Block Diagram of A7 Central Processor PCB*

- A clock chip and crystal oscillator that generate and control the clock signal to the microprocessor.
- Three 1 Mbit EPROMS that store operating firmware.
- A 1 Mbit RAM that stores calibration data, trace data, stored set ups, and unit identification information.
- Address latches and buffers that interface the microprocessor to the internal memory.
- Bi-directional data buffers that transfer data to/from the microprocessor and the internal address and data buses. Similar circuits transfer data to/from the external data, address, and interrupt buses that connect to the other PCB's in the 56100A.
- Interrupt control and vectoring circuits.
- A backup battery and control circuit that powers the RAM chip during power off conditions.

When the 56100A is powered up, the central processor is reset. It then performs the following initial operations:

- Runs the instrument self-test routine.
- Down-loads the display software to the A8 Graphics System Processor PCB.
- Sets up the unit with the last used front panel control configuration.
- Starts normal instrument operation.

GPIB Circuits

Four GPIB data bus transceiver chips and two GPIB controller chip comprise the GPIB interface circuits (Figure 5-2). The transceiver chips connect to the rear panel GPIB connector via the A9 Motherboard and associated connector cable assembly for the dedicated GPIB, while the system GPIB cable connects in the CPU PCB. The central microprocessor controls the GPIB controller and passes data to/from it via the internal data, address, and interrupt buses on the A7 PCB.

5-4 A8 GRAPHICS SYSTEM PROCESSOR PCB

The Graphic System Processor (GSP) circuits are located on the A8 PCB (Figure 5-3). These circuits comprise an intelligent subsystem that is loosely controlled by the A7 PCB Central Processor. It produces the video signals for the internal CRT monitor screen display. It also produces the data and control signals for the Centronics printer interface. There are no adjustments on this PCB.

Major GSP Circuits

The major circuit blocks that comprise the A8 Graphic System Processor PCB are:

- Graphics controller chip (34010) — this controller interprets the commands from the A7 PCB Central Processor and produces appropriate command signals and data streams that produce the desired CRT monitor display or printer output. The GSP controller communicates with the GSP memory, video output cir-

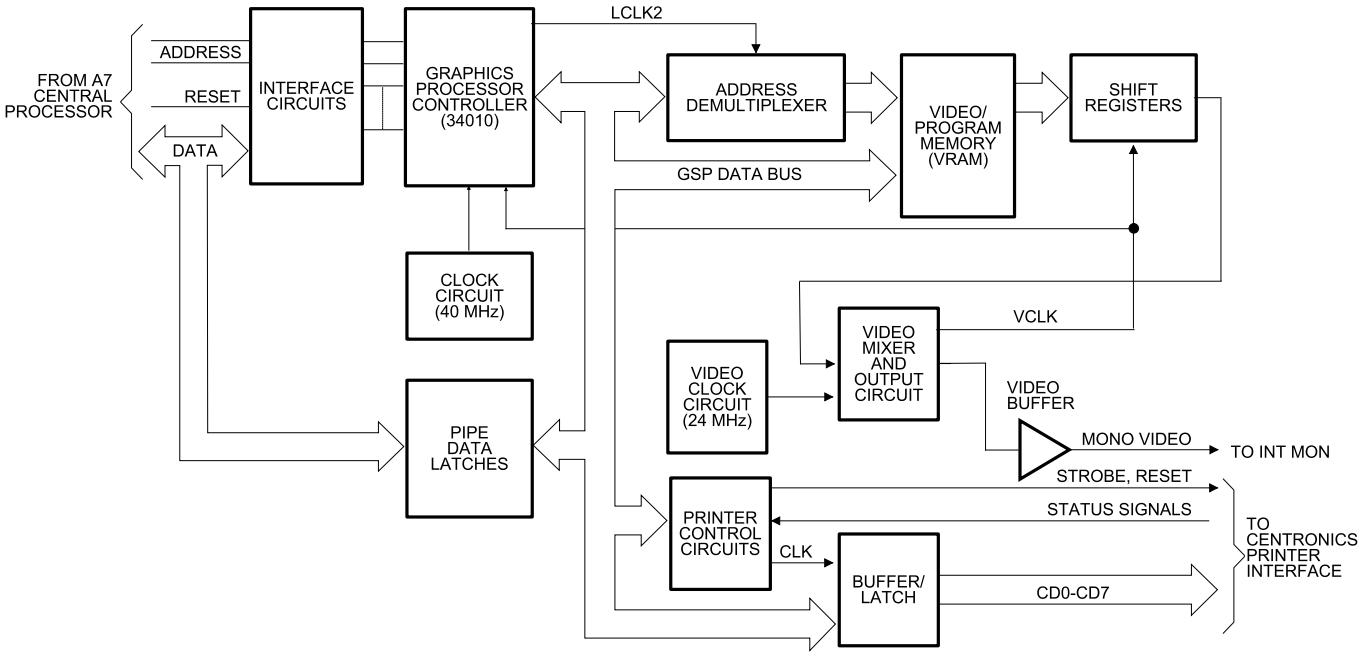

Figure 5-3. *Block Diagram of A8 Graphics System Processor PCB*

cuits and printer interface circuits via the internal GSP Data Bus (Figure 5-3).

- Clock Signal Generation — The 40 MHz clock chip produces the INCLK signal that is used by the GSP controller to derive all program related timing signals. The controller divides this signal by eight to produce the LCLK2 signal that clocks data into and out of the GSP memory. The controller also produces other timing and control signals related to this clock.

  The video clock oscillator and associated divider circuits produce the 6 MHz video clock signal,VCLK. This signal is used to establish the rate that the video information is clocked from the GSP memory to the video output circuits.

  NOTE

  For troubleshooting, all program-related cycles should be observed synchronized to LCLK2 (test point 2). All video cycles should be observed synchronized to VCLK (test point 3).

- Data interface circuits — these circuits interface the GSP processor to the data and address bus lines from the A7 central processor. The graphics processing control program is downloaded through this interface.
- Data "Pipe" — two latches form a data pipe that allows direct communication from the A7 central processor to/from the GSP processor via the GSP Data Bus (Figure 5-3).
- Video/Program Memory — four 256K x 4 Video Dynamic RAMs (VRAMs) comprise the memory for the GSP subsystem. This memory is used to store the GSP control program and the video data that will produce the CRT monitor screen display output.
- Video Output Circuits — Two shift registers, a video clock oscillator chip, a video mixer chip and a video amplifier/buffer circuit comprise the video output circuits. These circuits shift the video data out of the GSP memory and convert it into the mono-video signal for the internal CRT monitor.
- Centronics Printer Interface — A data buffer/latch, a printer interface controller chip and a

portion of a data latch comprise the interface circuitry for the Centronics printer interface. This circuitry provides the formatted data, data strobe, and control signals for the printer interface. It also receives and stores the status signals from the printer.

GSP Controller Operation

The GSP controller receives the graphics processing program down-loaded to it from the A7 Central Processor at power-up. It stores the GSP control program in the *high* memory locations of the GSP Video/ Program Memory and starts it on command from the central processor. (Low memory locations are used for video data.) The control program is run continuously until the 56100A is powered-down.

The GSP control program controls all aspects of the operation of the GSP subsystem, which include:

- Timing of communication operations from/to the central processor.
- Setting up the CRT scanning.
- Generating and maintaining the graphic elements of the CRT display.
- Formatting and controlling the data output to the Centronics printer interface.

A preliminary step performed by the program is the setup of timing information for the video output signals. This operation places certain control codes into the A8 PCB internal registers. (At execution time, the contents of these registers are processed in the same manner as memory location data.) These codes control internal clock dividers that generate the required Horizontal and Vertical Synchronization signals for the output video signal. The Video blanking signal is also generated in this manner.

The GSP control program causes the GSP controller to wait for instructions and data that are sent to it from the central processor via the pipe interface (Figure 5-3). The commands used by the central processor to control the GSP are high level commands such as **`draw line`** and **`write text`**. The GSP controller translates these commands into primitive instructions which it can directly execute. It then performs the necessary sub-tasks to produce the desired results.

For example, the command **`draw line`** performs the following operations: It generates primitive commands that instruct the GSP controller to produce a series of memory fetch cycles from the video data stored in the *low* memory locations of the GSP memory. After each fetch, it modifies the video data and returns it to memory. This process alters the contents of video memory so that when the memory contents are displayed on the CRT monitor, the desired line appears. The GSP controller performs these graphic memory fetch cycles interleaved with control program fetches from the *high* memory locations of the GSP memory.

The GSP control program does not control the overall content of the CRT monitor display — it produces graphic elements and puts them into video memory as instructed by the central processor. The central processor controls the content and placement of the graphic elements that make up the display. After the video information for a complete screen display has been built up in memory (as explained above), it is shifted out to the video output circuits.

Printer Interface Operation

The GSP processor sends formatted printer output data and control signals to the printer interface circuits via the GSP data bus. The printer interface controller chip provides the data strobe that clocks the output data from the GSP bus into the data buffer/latch (Figure 5-3). It also provides the LSTB (strobe) and PRINTER RESET signals to the printer. Along with associated data latch circuits, it receives the printer status signals and sends them to the GSP controller via the GSP bus.

Video Output Circuit Operation

The 24 MHz signal from the video clock oscillator is divided down and gated by divider circuits and the video mixer chip to produce the video dot-rate clock signal, VCLK. This signal and other clock signals from it are used to transfer the video data out of the GSP memory and shift it into the video mixer chip. These signals are mixed to produce a composite monochrome signal that is fed to the input of the video buffer amplifier. This amplifier boosts the signal to the 3 to 5V level required to drive the internal CRT monitor.

Internal CRT Monitor

The video and synchronization signals from the A8 Graphics System Processor PCB and the required DC power are fed to the CRT monitor by a cable assembly that connects to the A9 Motherboard PCB. The monitor is not field repairable and should be replaced with an exchange unit if defective.

NOTE

The adjustment potentiometers for these units are set at the factory and should require no further adjustment. Any adjustment of these potentiometers or of the CRT geometry magnets should *not* be attempted.

5-5 A1/A2 SIGNAL CHANNEL AMPLIFIER PCB FUNCTIONAL DESCRIPTION

The 56100A Scalar Network Analyzer contains two identical and interchangeable Signal Channel Amplifier PCBs, designated A1 and A2. The PCB in the A1 slot of the card frame processes the input signals from the R1 and R2 front panel connectors and the PCB in the A2 slot processes the signals from the A and B connectors.

Since the A1 and A2 circuit PCBs are functionally identical, only the operation of the A2 PCB will be described in this section. When working with the A1 PCB, simply substitute channel R1 for all references to channel A and substitute channel R2 for all references to channel B.

An overall block diagram of the A1/A2 Signal Channel Amplifier PCB is shown in Figure 5-FO1, located at the rear of this chapter. A block diagram of the A1/A2 Input (Switching) Module is shown below in Figure 5-4.

As shown in Figure 5-FO1, the A1/A2 PCB contains an input switching module, a gain switchable amplifier chain, a smoothing filter, a five-way multiplexer, and a sample-and-hold amplifier. The first three of these functions are controlled by data that is routed from the A3 Signal Channel Interface PCB via the quiet data bus and stored in latches on the A1/A2 PCB. Other signals from the A3 PCB directly control the five-way multiplexer and the sample-and-hold amplifier.

Input Switching Module

Detected dc voltages in the region of 1 microvolt to 2 volts from the external SWR Autotesters or detectors are routed via the front panel A and B connectors to the two 5-pin connectors located on the input switching module of the A1/A2 PCB. Channel A is connected to measurement channel 1 of the module (P1), and channel B is connected to measurement channel 2 (P2).

Refer to Figure 5-4; the Input Module contains switching field effect transistors (FETs) that multiplex the signal channel amplifier gain stages between the channel 1 and channel 2 inputs presented to the PCB. It also contains switching FETs to break the signal path from each input and present a short circuit to the input of the amplifier chain for the purpose of autozeroing. Figure 5-4 also shows the associated Input Bias Nulling feedback paths from the amplifier chain into the Input Switching Module. The Input Switching Module provides no amplification; it provides switching functions only.

The various switching functions of the Input Module are controlled by signals from latches U15 and U16. One output of octal latch U15 (pin 5) is used to

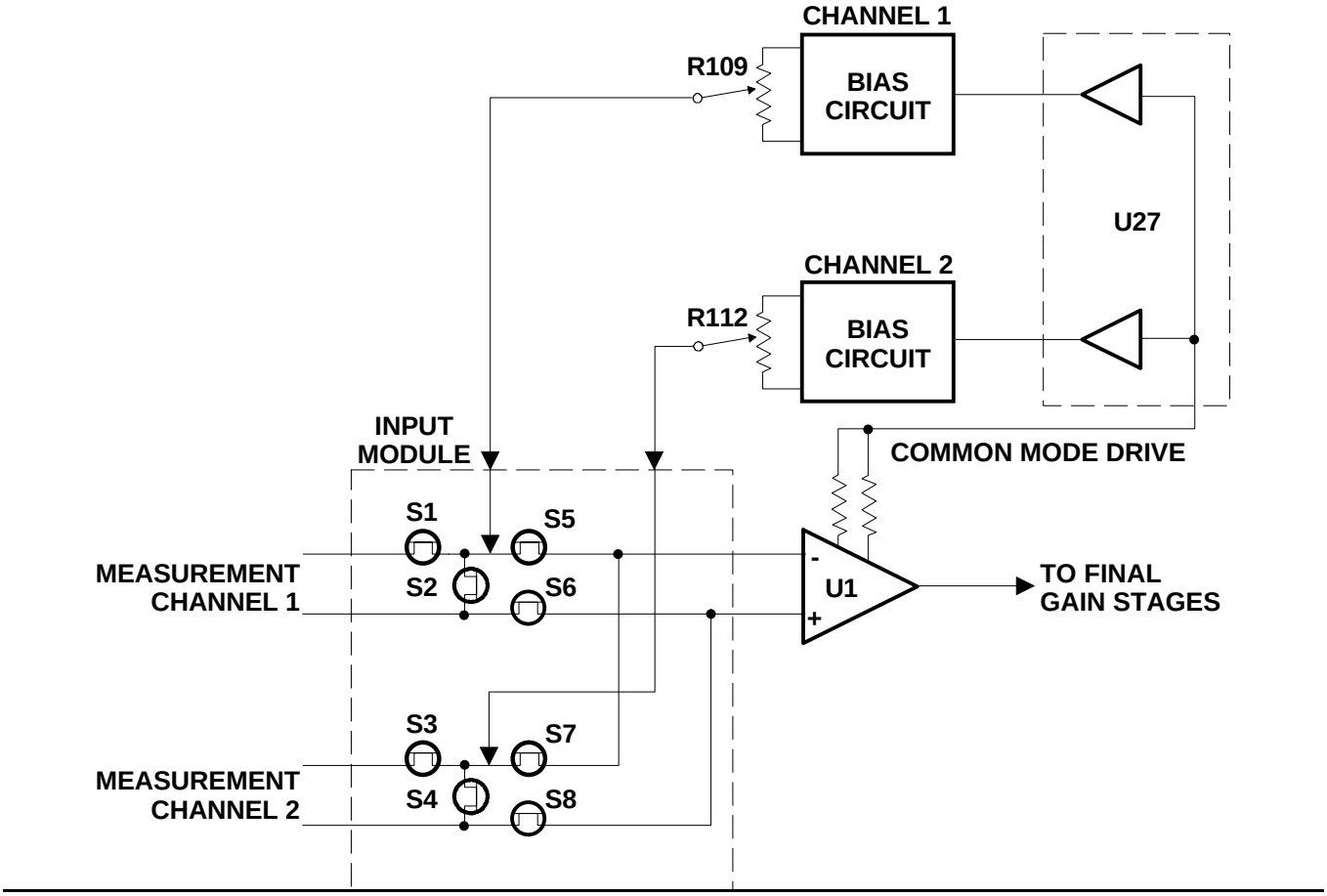

Figure 5-4. *Block Diagram of A1/A2 Input Module and Associated Circuits*

switch between measurement channel 1 and measurement channel 2. When the latch output is high, the voltage at pin 1 and pin 13 of U24 approaches +15V and switches S5 and S6 are turned on. The high output of U15 is inverted by hex inverter U21C which causes the voltage at pin 2 and pin 14 of U24 to approach –15 V. This ensures that switches S7 and S8 are turned off (open). This switching action connects measurement channel 1 to the input of U1, which is the first stage of the amplifier chain. When pin 5 of U15 is low, measurement channel 2 is connected to the input of the amplifier.

Hex latch output U16, pin 15, is used to select either the input signal from the front panel connector or a short circuit for each measurement channel, that is, connections to switches S5 and S7 as shown in Figure 5-4). When the latch output is high, the voltage at pin 1 and pin 13 of U23 approaches +15V and se-

ries-switches S1 (for channel 1) and S3 (for channel 2) are turned on. The high logic level from U16 is inverted by a section of hex inverter U21, and the voltage at pin 14 and pin 2 of U23 approaches –15V. This results in shunt-switches S2 and S4 being turned off (open). This switching action connects the measurement channel 1 and measurement channel 2 inputs through to the multiplexing switches (S5 & S7). When the latch output of U16 is low, the voltages at U23, pins 1 and 13, are reversed; S1 and S3 are turned off and S2 and S4 are turned on. This switching action produces a short-circuit at the input of each measurement channel that is connected through to the multiplexing switches.

Diodes CR1 through CR8 ensure that high positive FET drive voltages are not present to cause FET leakage current to be injected into the measurement path. U28 is a dual op-amp configured as a pair of followers driven from the input amplifier U1. They are connected to drive the source voltages of the switching FETs so that source and gate voltages are held to within about 0.65V when the FET is in the on state.

Amplifier Chain

The signal channel amplifier chain of the 56100A is a linear amplifier (the 56100A does not use log amplifiers). The log conversion process for channel 1/channel 2 measurement signals is performed by the 56100A CPU via use of a logarithmic look-up table.

The multiplexed channel measurement signal from the input switching module is applied to the differential inputs of instrumentation amplifier, U1, which is the first stage of the linear amplifier chain. An instrumentation amplifier is used for this stage because of its very high common mode rejection. This is necessary to extract the very small detected voltages from the high level of common-mode interference present on the input signals. The gain of U1 is programmable; it can be switched between four decade gains: X1, X10, X100, and X1000. The gain of U1 is controlled by outputs from U15 through the dual four-channel multiplexer, U2.

Capacitors C1, C2, and C3 filter out unwanted high frequency signals. Present at the input of U1, Potentiometer R40 is used to null out input circuit offset voltages generated by U1.

The last two stages of the linear amplifier chain consist of operational amplifiers U3 and U4. U3 is a non-inverting operational amplifier stage that is switched between a gain of X1 and X100 by two elements of quad FET switch U20A and U20B. The U4 amplifier stage is similar to that of U3; the gain of this stage is switched between X1 and X10 by the two remaining sections of U20.

Amplifier Signal Channel Nulling and Autozeroing

In spite of the use of low-offset/low-drift devices, some degree of offsets will occur in the outputs of the input switching module and instrumentation amplifier due to changes of time, temperature, and aging. To correct for these changes, Input Bias Nulling circuits are provided. The A1/A2 PCB also includes autozeroing circuitry that provides dynamic amplifier zeroing during the retrace portion of RF OFF DURING RETRACE mode of operation. (This is the preferred mode of operation.) Input Signal (Offset) Nulling circuitry is also included. It is used in the RF ON DURING RETRACE mode of operation.

Input Bias Nulling

Input bias currents—due to the switching FETs and the amplifier chain input connections—are small but significant for low level corrections. Correctional offsets for each channel are derived from floating 12 volt supplies and preset by R109 and R112. The 0 VOLT REF for these circuits is driven from the common mode voltage present on the input signal from the external SWR Autotester or detector (via U1).

Autozeroing Null

The preferred method of zeroing is with the RF output from the sweeper turned off during retrace, with the output of the SWR Autotester or detector still connected through the input module. In this state, the autozeroing circuit described below can null out residual thermal noise up to the point of the detector and, in addition, can zero out a certain level (approximately –40 dBm) of wideband noise from the sweeper.

The Autozero DAC circuit is comprised of U7, which is controlled by latched outputs from U8, U9, and U10. The output of this circuit is adjusted by the A7 central processor by writing correction values to the 10-bit digital to analog converter (DAC) U7. Six-bit latches U8, U9, and U10 latch the data for the DAC. Because the data bus is only 8-bits wide, the most significant 8-bits are latched onto U8 and U9, fol-

lowed by the remaining 2-bits onto U10. The reference voltage to DAC U7 is set by divider R82 and R101, and is approximately 75 mV. The current output of the DAC is converted to voltage by one-half of the dual operational amplifier U6. It is then doubled and offset by the reference voltage (by the other half of U6). Hence, the output of the autozero circuit can be varied between approximately ±75 mV in 1024 steps. This variable autozeroing voltage is applied to the output offset voltage pin of instrumentation amplifier U1, thus enabling any residual output offset voltage from the amplifier chain to be corrected.

Input Signal (Offset) Nulling
The input signal nulling circuitry is another form of autozeroing circuitry that is used when the 56100A is being used in the RF ON DURING RETRACE mode of autozeroing. During this mode, the sweeper RF power is not being turned off during retrace, so there is a non-zero output voltage from the external SWR Autotester or detector; therefore, the residual offset voltages from the amplifier chain must be nulled by another means.

To use this mode of operation, the LOW LEVEL TRIM procedure must first be selected from the front panel calibration menu. When this operation is selected, the operator is instructed to remove the RF power input to the SWR Autotester or detector. The output of the SWR Autotester or detector is switched through to the amplifier chain input for autozeroing by DAC U7, just as it would be when zeroing with RF OFF DURING RETRACE mode of operation.

The input switching module switches a short circuit to the input of the amplifier chain and injects offset nulling signals for Channels A/B from DAC circuits U25 and U26.

Without varying the autozero data, the null circuit is used to apply offsets to the input module circuitry to make the noise floor identical to that achieved from the SWR Autotester or detector in the RF OFF DURING RETRACE state. Thus we now have an artificial reference with which to compare the output of the amplifier chain for autozeroing during the RF ON DURING RETRACE mode of zeroing.

Smoothing Filter

The smoothing filter consists of a simple, switched, passive RC filter network. This circuit is comprised

of R48 and one (or none) of capacitors C32, C33, C34, and C35 as selected by quad FET switch U5. When *no* smoothing is selected from the instrument front panel, no smoothing capacitance is used and the frequency response is that set by the preceding linear amplifier stages. If *minimum* smoothing is selected, then capacitors C33 and C34 provide the extra filtering (C34 for channel A and C33 for channel B). The use of individual switching capacitors for each channel avoids lengthy recovery times. If *maximum* smoothing is selected, the extra filtering is provided by capacitors C32 and C35 (C32 for channel A and C35 for channel B).

This 6-bit latch sets the level of smoothing of the signal channel. To avoid lengthy recovery times, separate smoothing capacitors are provided for each of the two multiplexed inputs of each signal channel. Additionally, this latch controls whether the signal channel's input module is switched to the dummy detector position or to the actual detector input.

Multiplexing and Sample/Hold

The dc voltage output from the signal channel linear amplifier chain is fed to sample/hold amplifier U13 via a five way multiplexing circuit consisting of four-pole FET switches, U11 and U12. The first position of the multiplexer circuit is used to switch the (multiplexed) channel 1/channel 2 signal from the smoothing filter to the input of the sample and hold amplifier, U13. The other four positions of the multiplexer are used to switch the log conformity and temperature compensation correction voltages from buffer amplifiers U19A, U19B, U19C and U19D to the input of U13.

The five select lines to the multiplex circuit, and the sample/hold control line for U13 come from the A3 Signal Channel Interface PCB. Capacitor C36 is the hold capacitor for U13. The output of U13 is routed via the A9 Motherboard PCB to the A3 PCB.

Log Conformity/Temperature Resistor Sensing

Log conformity/temperature corrections for the SWR Autotesters or detectors used with the 56100A are performed by the instrument software using the information available from the log conformity resistors and thermistors contained within these external devices. The values of these resistances are converted to voltages by connecting them to form voltage dividers. The reference voltage source for these voltage dividers is generated by the 5.6V zener diode CR9. The

output voltage from each divider circuit is fed via a unity gain, high impedance buffer amplifier to the five way multiplexer described above. (These buffer amplifiers are contained in the quad op-amp U19.) To achieve the high accuracy required for the log conformity correction, potentiometer R62 and R64 are included in the log conformity potential dividers; R62 provides adjustment for channel A and R64 provides adjustment for channel B.

Power Supplies

The ± 15V and the +5V supplies to the A1/A2 Signal Channel Amplifier PCBs are filtered locally on the board by LC π network filters to give increased immunity to noise.

The +5V supply to U2, U5, U11, and U12 is derived from the +15V supply by voltage regulator VR1. This gives increased decoupling over the alternative of using the potentially noisy digital +5V supply.

Digital Decoding Circuitry

Most of the control signals from the CPU (A5) PCB that control the Signal Channel Amplifier (A1/A2) PCBs are sent via the A3 PCB onto the Quiet Data Bus to latches contained on the A1/A2 assemblies. Signal data activity on this bus is managed so that there is minimum disturbance to the sensitive analog circuitry of the A1/A2 PCB during actual signal measurement.

The remainder of the digital control lines for the A1/A2 PCBs are decoded on the A3 Signal Channel Interface PCB, from processor bus signals. This decoding is considered in more detail in the description of the A3 PCB.

5-6 A3 SIGNAL CHANNEL INTERFACE PCB FUNCTIONAL DESCRIPTION

The 56100A contains one Signal Channel Interface PCB (A3). This PCB contains decoding circuitry to control the various functions of the A1 and A2 signal channel amplifier PCBs, and performs the analog to digital conversion of the signals from the A1/A2 PCBs for interfacing with the A7 Main CPU PCB.

The A3 PCB also contains an analog channel that is used to digitize the 10V sweep ramp signal from the A4 sweeper interface PCB. Refer to the overall block diagram (Figure 5-5) while reading this description. A parts list, along with parts locator and schematic diagrams are located in Appendix A-Maintenance Data.

Input Multiplexing Circuit

Analog signals from the A1/A2 Signal Channel Amplifier PCBs and the ramp output of the A4 Sweeper Interface PCB are input to the edge connector of the A3 Signal Channel Interface PCB. Quad FET switches U1 and U2 are configured as a multiplexing circuit to select the desired analog signal to be digitized. The sense and return paths of each signal are switched through the same FET switch (U1 or U2) in order to achieve a similar series resistance within each input path. This is required to maintain the common mode rejection characteristics of the following differential amplifier stage (U3).

The fourth multiplexing switch position is connected to the circuit analog ground. This position is used during instrument self test to inject a reference offset at the input of the analog to digital converter so that its operation can be verified.

The input multiplexing circuit comprised of U1 and U2 is controlled by four of the outputs of octal latch U17. The state of these U17 outputs can be monitored by probing test points TP11 to TP14. These test points correspond to the analog input signals as follows:

- TP11: A2 Analog
- TP12: 0V Reference
- TP13: A1 Analog
- TP14: Ramp Out (from A4)

The +5V supply for U1 and U2 is derived from the +15V supply using the three-terminal voltage regulator VR2. This technique helps to decouple this circuitry from the potentially noisy +5V supply used for digital circuitry.

Op Amp Stages U3 and U4

Integrated circuit U3 is a X1 gain operational amplifier that has low-noise/low-offset voltage characteristics. It is used in the elementary single op-amp differential amplifier circuit configuration to achieve common mode rejection between the signal channel interface and the circuits feeding it.

The output of U3 goes to U4, a X1 gain inverting buffer stage. This stage inverts the negative going signal at the output of U3 in order to present the analog to digital converter (ADC) with a positive go-

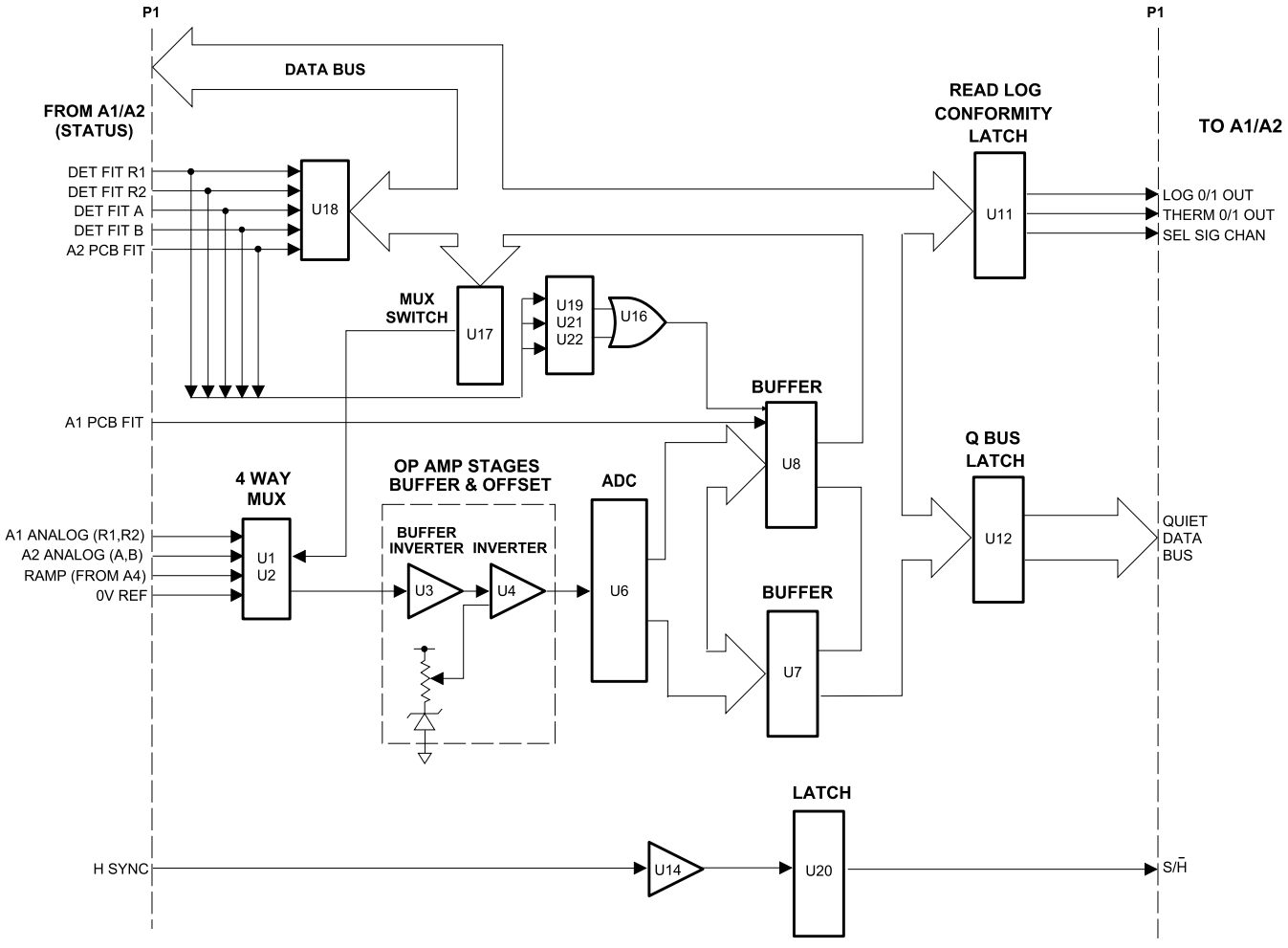

Figure 5-5. *Block Diagram of Signal Channel Input Switching and Amplifier Chain Circuits*

ing signal (the ADC is configured in its unipolar mode of operation). In order to ensure that the signal at the ADC input is actually positive, an offset voltage of approximately 50 mV is applied to the non-inverting input of U4. This voltage is set by the potential divider R14 and R7 connected across zener diode CR1. The input offset results in an U4output voltage offset of 2 x V_{offset}, i.e., 100 mV. The output of U4 is applied to the input of the ADC chip, U6.

Analog to Digital Conversion

The analog-to-digital conversion circuit (ADC) is comprised of U6, a 12-bit resolution device that is configured to accept an input voltage range of 0 to 10V. This device requires plus and minus 15V supplies, as well as a +5V supply. The +5V supply for U6 is derived from the +15V supply rail using VR1, a three terminal voltage regulator. The ADC conversion process is initiated by the STROBE ADC NIBBL signal from U10, which is an eight-line decoder chip.

The A7 Main CPU PCB communicates with the A3 PCB over an 8-bit data bus. The 12-bit output of the ADC requires two separate read cycles for a complete read operation. At the beginning of the first read cycle, octal tri-state buffer U7 is enabled by a decoded line from U10 to read the eight most significant ADC data bits, D11 to D4. Octal tri-state buffer U8 is then enabled by another decoded line from U10 to read the four least-significant bits of ADC data, D3 to D0. These appear on bits D7 to D4, respectively, of the 56100A data bus. The other four sections of buffer U8 are used for the A1 PCB fitted data bit, the output of the detector fitted latch, the status of the synchronized sample/hold latch and the status of the ADC.

Sample/Hold Control Circuit

The signal channel interface PCB outputs a common sample/hold control line to the sample and hold amplifiers contained on the signal channel PCBs. The sample/hold signal can be derived using one of two methods.

The primary method is to allow the CPU to directly set the sample-and-hold signal, as required. When this method is used, pin 2 of U17 is set high. This enables one input of two-input OR gate U15C; therefore, the output of this gate will be high regardless of the level of the other input. The output of U15C is connected to one input of two-input AND gate U13C.

When enabled by U15C, the output of U13C follows the state of the other input that is derived from the output of one of the D-type latches contained within U20. The output of gate U13A is the S/H (sample/hold) signal and is set high or low (high for sample, low for hold) by writing to latch U20. This is accomplished via the STROBE ADC BYTE output from the eight-bit decoder U10 In conjunction with data bit D0.

The other method of controlling the S/$\overline{H}$ signal is to synchronize it with the rising edge of the horizontal synchronization pulse of the internal monitor (CRT) assembly. This is particularly advantageous for low level signal channel signals. (Shortly after the edge of the synchronization pulse, a large pulse is radiated from the CRT. This radiated pulse could affect the accuracy of a low-level signal being read if the channel is still sampling data.)

Detector Fitted Circuitry

As shown in Figure 5-5, each signal channel amplifier PCB feeds status information to the A3 Signal Channel Interface PCB. This status information indicates which external detectors are connected to the instrument front panel and whether each signal channel PCB is plugged into its edge connector. All but one of these status signals are read using octal buffer U18. The output of U18 is controlled by eight-line decoder U9. The remaining status signal, A1 PCB FIT, is read by one of the spare data bits of octal buffer U8.

In addition to being fed to buffer U18, the DETECTOR FITTED signals are latched by U19, U21 and U22. The outputs of these latches go to the 6-input OR gate formed by U15A, U16B, U16C, U16D and U15B. If any of these latches are set, a high logic level occurs at the DETECTOR FITTED output of the OR gate and is routed to one of the spare bits of the octal buffer U8. This signal is read by the CPU, along with the least-significant four data bits from the ADC. Because of the DETECTOR FITTED signal, it is not necessary for he A5 central processor to continuously poll buffer U18 to determine when a new SWR Autotester or detector has been connected to the 56100A. This signal remains high until the latches U19, U21 and U22 are reset by the CPU by pin 5 of latch U17.

Signal Channel Multiplexer Control

Five outputs of octal latch, U11, are used as control signals for the five-way multiplexer contained on each signal channel amplifier PCB. These control signals are paralleled to each PCB, so that the multiplex circuits are switched at the same time.

Quiet Data Bus

Octal buffer U12 is enabled by any one of the signal channel select lines from U9 via AND gate U5. In this way, the noisy CPU data bus is only connected to the signal channel PCBs when it is required to write to them. Thus, the sensitive analog circuitry contained on the signal channel amplifier PCBs is isolated from the general background noise level of the instrument data bus.

Power Supplies

The plus and minus 15V and the plus 5V supply rails to the A3 Signal Channel Interface PCB are all filtered locally on the PCB by LC pi-network filters to obtain increased immunity to noise. Voltage regulators VR1 and VR2 locally regulate from the +15V supply to provide +5V supplies to the analog function integrated circuits, U1, U2 and U6.

Digital Decoding Circuitry

The digital control lines for the A3 signal channel interface and the A1/A2 signal channel PCBs are decoded from CPU control lines by the two eight-line decoder integrated circuits U9 and U10. Some further decoding is implemented on the signal channel PCBs using a combination of the CPU control lines and the PCB select line from the A3 PCB.

5-7 A4 SWEEPER INTERFACE PCB FUNCTIONAL DESCRIPTION

The purpose of this PCB is to provide an interface for the control signals that operate between the 56100A and the associated swept signal source. All the signals required to allow the 56100A to operate with a wide range of swept signal sources are provided. The A4 PCB contains both analog and digital circuitry which are physically separated. However, it is more logical to consider the whole as a series of functional circuit blocks; some containing analog circuitry, some containing digital circuitry, and some containing both analog and digital circuitry. Refer to the block diagram (Figure 5-6) while reading this description.

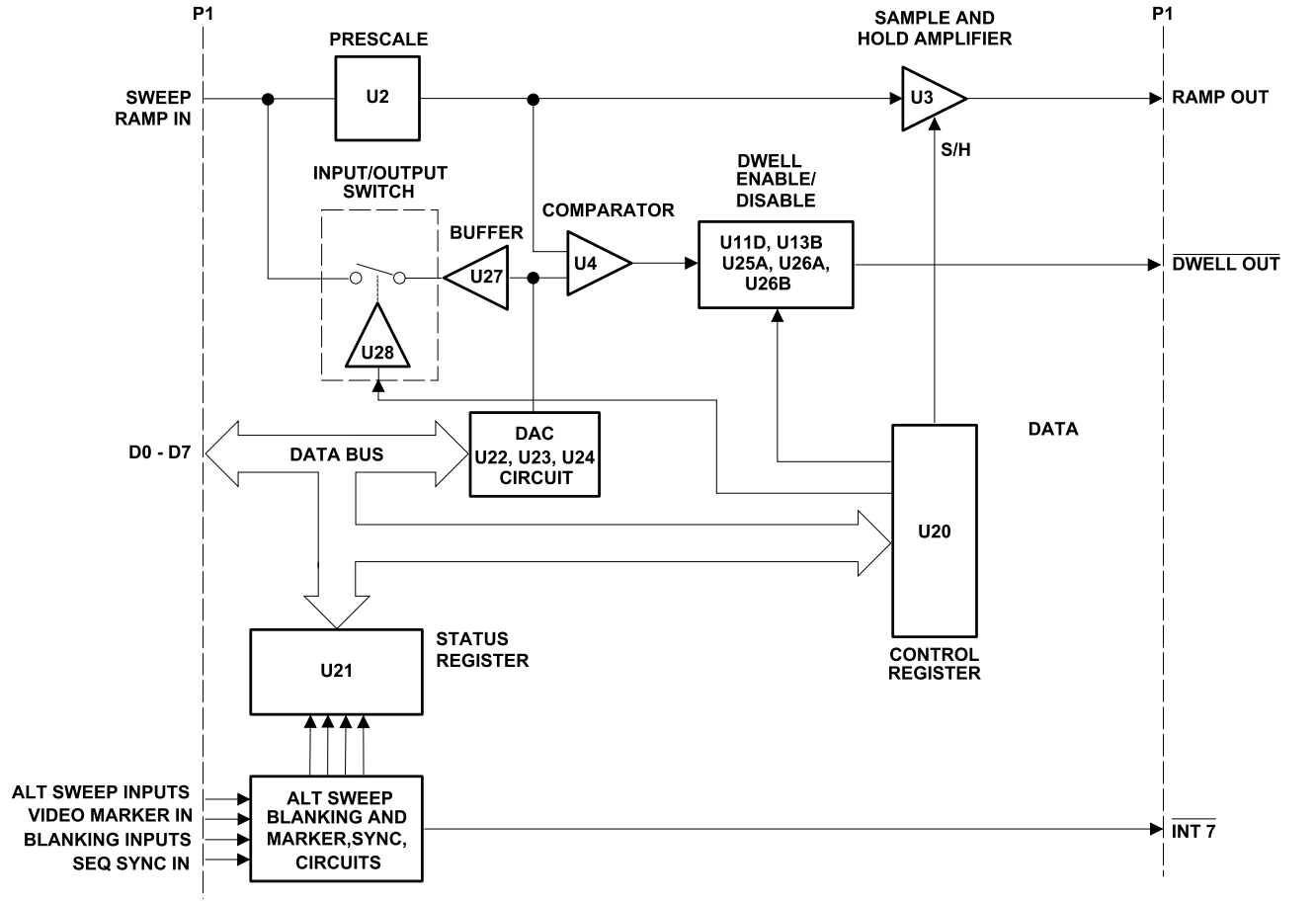

Figure 5-6. *Block Diagram of A4 Sweeper Interface PCB*

Sweep Ramp Normalizer Circuits

Integrated circuit U2A and resistors R4, R5, R6, R7, R8 and R77 form an inverting, differential input, buffer amplifier with an overall gain of approximately 0.8. Attenuation is provided by resistors R4 and R6; this attenuation is necessary to allow the use of some swept signal sources that have sweep ramps that exceed +10V.

Integrated circuit U2B and resistors R9, R10, R11, R12 and R13 form a X1 gain inverting amplifier with a small amount of output offset. This offset, which is set by R12 and R13, is introduced to allow for a possible negative offset on the input ramp signal. Potentiometer, R10, is included in the feedback loop of U2B to allow adjustment of the overall gain of the two stages.

Note that although the gain at the inverting input of U2B is X1, the gain at the non inverting input is X2. Therefore, the offset voltage set by R12/R13 is amplified by a factor of two. This offset provides an undervoltage range of approximately 1V.

Integrated circuit U3 is a sample and hold amplifier; the output of this circuit is connected via the motherboard to the Signal Channel Interface (A3) PCB. This configuration provides an alternative method of tracking the sweep ramp input.

10V Reference

Op amp U1, diode CR1, and resistors R1, R2, and R3 form a 10V reference voltage source. CR1 is in fact an integrated circuit with the characteristics of a high-grade 5.0V zener reference diode. U1 provides buffering and a gain of X2 to produce an output voltage of approximately 10V that is stable over time and temperature. Stability is further improved by providing the current for CR1 from the output of op amp U1. Op amp U1 is powered from a single +15V supply to ensure that the reference always starts up in the positive direction.

Digital to Analog Converter

ICs U22, U23, and U24 form a 12-bit digital to analog converter. In the normal mode of operation, this circuit is used to produce the operating reference voltage for the sweep ramp comparator circuit. When the Ramp Output Mode of operation is selected by the user, this circuit generates the ramp signal that is output via the HORIZONTAL INPUT/OUTPUT connector.

The negative-going DAC output from U24 is a fraction of the 10V reference voltage. The actual value of this output is determined linearly by the magnitude of the 12-bit data word loaded into U23 from the A5 CPU PCB. Since the data bus on the A4 PCB is only 8-bits wide, U22 is used to temporarily store the lower 4-bits of the 12-bit data word received. These 4-bits are first loaded into U22. The output of U22, combined with the upper 8-bits from the data bus, forms the 12-bit data word loaded into U23.

The DAC output from U24 is inverted by op amp U27, which is configured as a X1 gain inverting amplifier. When Ramp Output Mode is selected by the user, the output of U27 is fed via analog switch U28A and R85 to the HORIZONTAL INPUT/OUTPUT connector (via the A9 Motherboard). This configuration allows the user to drive external test circuitry using the DAC output (sweep ramp) signal. This signal is controlled by sequentially stepping the DAC through its 0Vto 10V range, as required.

Sweep Ramp Comparator Circuit

Integrated circuit U4 is a high speed, precision voltage comparator. This circuit monitors the voltage resulting from the summation of the normalized ramp voltage and the DAC voltage and sets a flag when this resultant voltage is zero.

The tracking of the input sweep ramp signal is accomplished as follows: the desired voltage level corresponding to a data collection point is loaded into DAC, U23. The negative voltage output from U23/U24 is then summed with the positive ramp voltage from U2B via resistors R15/R16. Resistor R18 provides the ramp comparator with hysteresis by providing positive feedback.

At the beginning of the input ramp waveform, the ramp voltage will be less than that of the DAC voltage and the resultant will be negative; this will cause the output of the comparator to be at logic low

level. As the ramp voltage rises, the summed voltage becomes less negative until the ramp voltage is equal in magnitude to the DAC voltage. At this point, the comparator triggers and the output goes to the logic high level. This RAMP MATCH signal is fed via gates U25A /U11D to open collector driver U14A. The output of U14A is the DWELL OUT signal to the swept signal source.

When the $\overline{\text{DWELL OUT}}$ signal goes low, the swept signal source is stopped. The 56100A and the swept signal source remain in this state during the time that a measurement is taken. The $\overline{\text{DWELL OUT}}$ signal is released by loading the next higher data collection point into the DAC. The output of the comparator then goes low and the whole process is repeated until the end of the sweep. U25A is used to invert the sense of the comparator output so that the ramp voltage can be tracked during both forward sweep and retrace phases. Gate U11D is also used to enable and disable the $\overline{\text{DWELL OUT}}$ signal via pin 19 of U20.This signal can also be set independently from the control register U20, pin 15, via gate U13B.

Sequential Sync Normalization

The Sequential Sync signal provided by some swept signal sources may combine frequency marker pulses as well as the various blanking pulses. This circuit is designed to separate the marker pulses, if present, from the blanking pulses. For this circuit to operate correctly, the blanking pulses must be positive and the marker pulses must be negative. Resistors R31, R32, and integrated circuit U6 form a X1 gain, inverting buffer. Negative pulses from the output of this buffer (i.e., blanking pulses) are passed via a level translator, R39, R40, and CR9, to gate U11C. The output of U11C is the Composite Blanking signal that is routed to the status register and to flip flop U17A via gate U15B. The output of U17A is OR'ed with several other signal lines to form the interrupt signal $\overline{\text{INT7}}$.

Any positive pulses at the output of U6 are fed via R33 and CR8, which block negative signals, to voltage comparators U7C and U7D. U7C has a threshold voltage of 3V and detects Marker pulses. U7D has a threshold voltage of 6.5V and detects Active Marker pulses. Apart from the difference in thresholds, the action of the two circuits is identical; therefore, only the Marker circuit will be described.

Device numbers for the Active Marker circuit are shown in brackets.

The output of the comparator remains off and is pulled high by R37 (R43) until the input signal exceeds the threshold voltage. At this point the comparator turns on and its output goes low. R38 (R44) provides positive feedback for hysteresis to increase noise immunity. The comparator output goes to gate U11A (U11B) where it is conditioned. From there it goes to the clock input of flip flop U15A (U15B). The output of the flip flop goes to the status register and to gate U15D where it is OR'ed with other signals to produce INT7. Resistor R34 ensures that the signal inputs of the comparators do not float up past the thresholds when no signal is applied.

Video Marker Normalization

This circuit provides an alternative means of inputting frequency marker information for those swept signal sources which have a separate Video Marker output. It does not differentiate between Active and non-Active markers and will accept both positive and negative marker pulses. Resistors R19, R20, zener diodes CR2, and CR3 provide overvoltage protection to the non inverting, X1 gain, buffer U5A. The protection circuit limits the voltage applied to the U5A to approximately +10V and -10V. Inverse parallel connected diodes CR20 and CR21 fed the output of U5A to the input of the high gain inverting amplifier U5D. The output voltage of U5D is limited to about 5.1V.

This stage converts an input pulse of whatever shape or amplitude to a 5.1V square wave pulse of opposite polarity. Since this stage has high gain (approximately 50), even small signals at the input will produce 5.1V pulses at the output (including noise). The two diodes CR20 and CR21 block signals of less than about 0.6V thus reducing the likelihood of spurious output pulses due to low level noise.

Op amps U5C/U5D along with resistors R23, R24, R25, R26, R27, R28, diodes CR6 and CR7 form a full wave rectifier (absolute value) circuit which has an overall gain of +X1 or -X1. A signal of either polarity applied to the input will appear at the output with the same amplitude, but with a fixed, positive polarity. The purpose of this circuit (along with the two preceding stages) is to convert input marker pulses

of any shape size or polarity to uniform positive polarity square-wave pulses with an amplitude of 5.1V.

The marker pulses from the absolute value circuit are detected by a comparator that has a threshold voltage of approximately 3V. This comparator circuit is formed by U10C, R30, R74, R75, and R76. The output of this circuit goes low (0V) when the input exceeds the threshold; otherwise it is held high (5V) by R29. Hysteresis for this circuit is provided by R74. The output of the U10D is OR'ed into the Sequential Sync circuit by gate U11A.

Retrace Blanking and Bandswitch Blanking Normalizer Circuits

The Retrace and Bandswitch Blanking Normalizer circuits are identical in form and function. Therefore only the Retrace circuitry will be described here; corresponding Bandswitch Blanking circuit component numbers appear in brackets. Resistors R45, R46 (R55, R56), zener diodes CR10, and CR11 (CR14, and CR15) form an input protection circuit that limits the signal applied to op amp U8A(U8B) to approximately +10V and -10V. Op amp U8A (U8B) is configured as a X1 gain, non inverting buffer amplifier.

The output of the buffer is connected to an absolute value circuit comprised of U9B/U9A ,R47, R48, R49, R50, R51, CR12 and CR13 (Bandswitch Blanking circuit: U9C/U9D, R57, R58, R59, R60, R61, CR16 and CR17.) The action of this circuit is identical to that of the absolute value circuit described in the Video Marker section above.

The output of the absolute value circuit is monitored by the voltage comparator circuit U7A (U7B). This circuit has a threshold voltage of approximately 2.5V fixed by R52 and R53 (R52, R53). The output of this comparator goes low (0V) when the input exceeds the threshold otherwise it is pulled high (5V) by R54 (R62). The comparator output is routed via gate U12A (U12B) to the status register.

The outputs of gates U12A and U12B, in addition to being routed separately to the status register, are OR'ed together by gate U15A. The resulting composite signal is then OR'ed with the MODIFIED COMPOSITE BLANKING signal from the Sequential Sync circuit by gate U15B.

Alternate Sweep Normalizer Circuits

The Alternate Sweep Enable Normalizer and Alternate Sweep A/B Normalizer circuits are identical. Therefore only the Enable Normalizer circuit will be described here. The A/B circuit component numbers are shown in brackets. The input signal is fed via resistor R63 (R66) to the voltage comparator U10B (U10A). The threshold voltage of this circuit is set to approximately 2.5V by resistors R52 and R53 (R52, R53). Resistor R64 (R67) prevents the comparator's signal input from floating above the threshold voltage when no signal is applied. The comparator output goes low (0V) when the input exceeds the threshold; otherwise it is held high (5V) by R65 (R68). This signal is fed via gate U12D (U12C), to the status register.

5-8 FRONT PANEL ASSEMBLY A1 & A2 FRONT PANEL PCBS

The A1 and A2 Front Panel PCBs are mounted on the rear surface of the front panel and contains the control key switches and indicator LED's for the main portion of the front panel. In all, 45 switches and 11 LED's. The switches are of single pole, membrane construction. The contacts of each switch are formed by two interleaved, gold plated PCB traces directly underneath the switch membrane. Depressing the control key cap flexes the membrane and forces it into contact with the PCB traces, thus closing the switch. The operation of the switch interface circuits is described in a following paragraph.

Keyboard Interface Circuits

The switches on the A1 PCB are connected into a two-dimensional matrix consisting of eight X-lines and eight Y-lines (Figure 5-7). Each switch point forms a unique X/Y coordinate (i.e., address); however, only 45 of the 64 possible X-Y combinations are used for switch positions. Closing any switch connects one of the Y-lines to one of the X-lines.

The switch controller/decoder circuit on the A2 PCB sequentially pulses the eight X-lines and also monitors each of the eight Y-lines for the presence of pulses. A pulse detected on a Y-line signifies a switch closure, which causes the controller/decoder circuit to send a Control Key Interrupt signal to the A7 Cen-

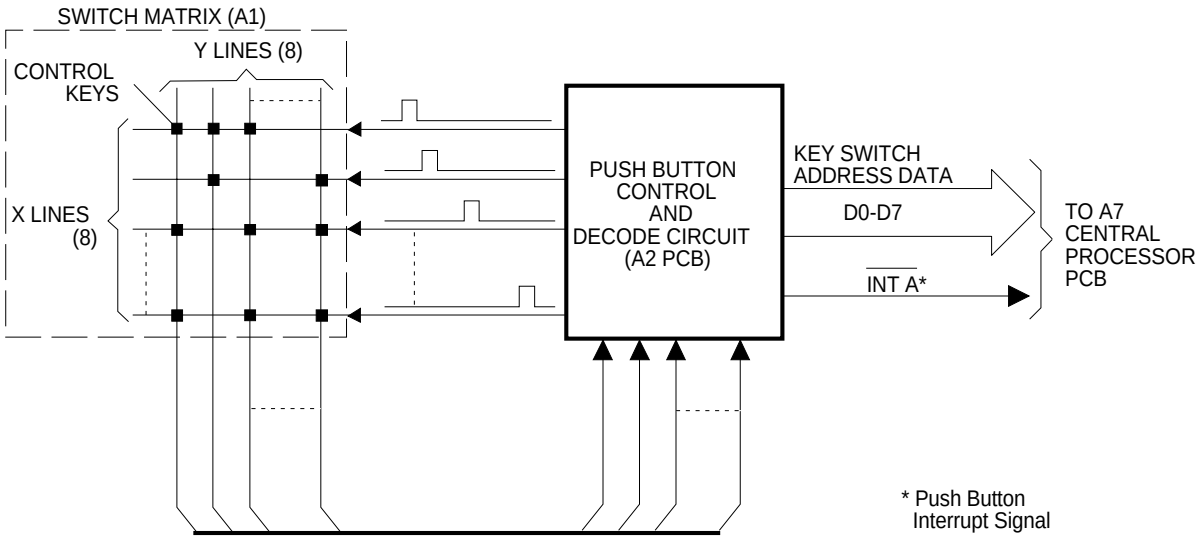

Figure 5-7. *Control Key Matrix and Decode Circuits Block Diagram*

tral Processor. The unique switch address determined by the X-line/Y-line combination is output from the controller/decoder circuit as a data byte onto the Central Processor Data Bus. Upon receiving the interrupt, the Central Processor reads the address byte to determine which key was pressed.

LED Indicator Latch Circuits

The 11 LED indicators located on the A2 PCB are controlled by latches on the A2 PCB (Figure 5-8). The Central Processor causes an individual LED indicator to be lit by writing a logic **zero** into the latch bit associated with the selected LED. A control strobe from the control decode circuit clocks the data into the data latches. Each latch output line contains a current limiting resistor for the associated LED.

Data Entry Knob Interface

The Data Entry Knob is fixed to the shaft of a small DC motor that is used as a generator. When the knob is rotated, the motor produces a DC voltage which is proportional to the speed of rotation. The polarity of the voltage indicates the direction of rotation of the knob. The output of the motor is connected to the Data Knob Interface Circuits (Figure 5-7). The input portion of these circuits consists

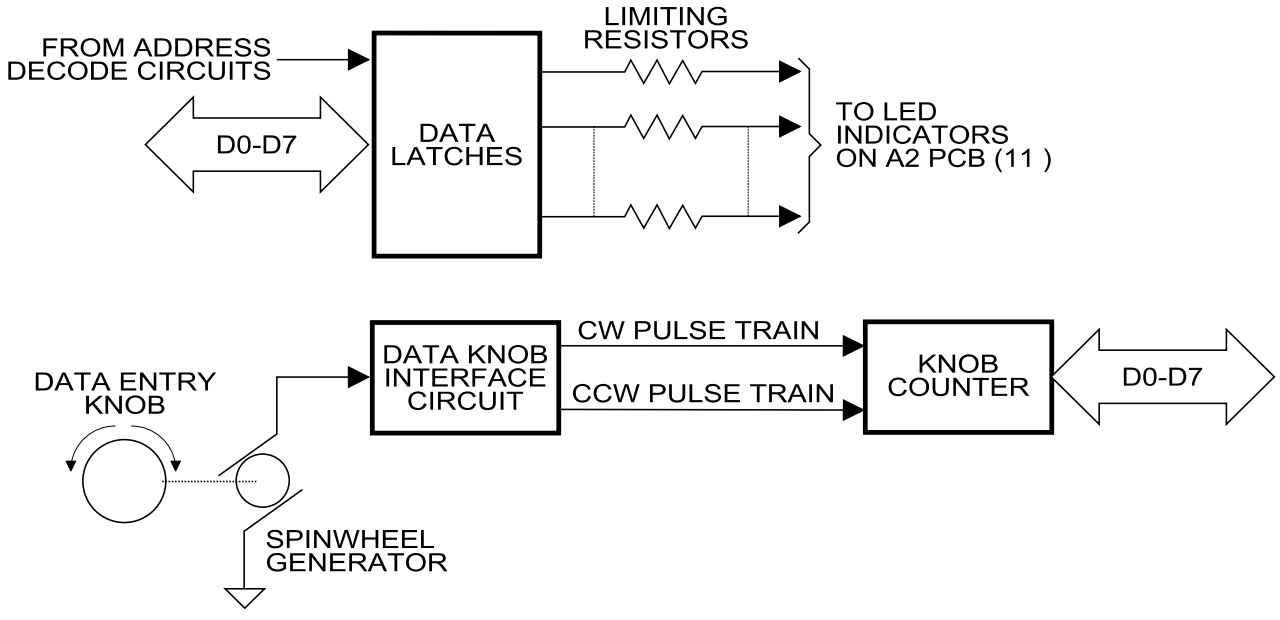

Figure 5-8. *LED Indicator and Data Entry Knob Interface Circuits Block Diagram*

of two comparator circuits: one circuit that produces a pulse train for clockwise knob rotation, and a second circuit that produces a pulse train for counter-clockwise knob rotation.

The pulse rate of the CW and CCW pulse trains is determined by the rate of knob rotation. These signals are fed to the Knob Counter Circuits, which are read by the CPU at a fixed rate.

CPU Interface Circuits

The Address Decode Circuits located on the A2 PCB decode the address lines of the Central Processor Data Bus to produce strobe signals that control the interface circuits located on the A2 PCB. These signals clock data from the data bus into the Keyboard Interface Circuit and the LED Indicator data/driver latches. They also control the clocking of interrupt signals and keyboard address data onto the data bus.

5-9 A9 MOTHERBOARD PCB FUNCTIONAL DESCRIPTION

The A1-A4, A7-A8, Front Panel Assembly A2 PCB, and A12 assemblies of the Model 56100A are all interconnected via edge connectors mounted on the A9 Motherboard PCB. The internal CRT Monitor Assembly and the Fan Assembly are all connected to the remainder of the 56100A circuitry via cables that plug into the motherboard.

The motherboard routes all dc power from the A12 Power Supply PCB to all other PCBs. It provides the distribution paths for the main data bus from the A7 central Processor PCB to the A3, A4, A8, and Front Panel A2 PCBs. It also connects the quiet data bus from the A3 Signal Channel Interface PCB to the A1/A2 Signal Channel Amplifier PCBs and provides all other signal paths between the PCB assemblies.

A list of PCB cable connectors is given in Table 5-1.

Table 5-1. *A9 Motherboard PCB Cable Connectors*

Connector	Cable Destination
J1	A2 Front Panel Interface PCB
J2	Internal Monitor
J3	PSU
J4	FAN
J5	AUX I/O rear panel connector
J6	Dedicated GPB
J7	Parallel Printer
J8	Rear panel BNC connector
J9	Not used

5-10 A12 POWER SUPPLY PCB FUNCTIONAL DESCRIPTION

The A12 Power Supply PCB assembly provides seven regulated output voltages. These supply voltages are listed in Table 5-2. A

General

The ac line power input to the A12 PCB assembly is routed through the line voltage selector module located on the rear panel. This module contains a line fuse and a line filter and allows the use of either of the four international line voltages: 100, 120, 220, and 240 Vac.

Two cable harnesses distribute the ac line power from the line voltage selector module; one is routed to the front panel mounted line ON/OFF switch, and the other goes to the primary windings of the toroidal transformer via an over-temperature thermostat that is mounted on the power supply heat sink.

The secondary windings from the transformer are routed though another harness to the rectifier bridge inputs of the ±15V and +12V power supplies on the A12 PCB assembly. This harness is connected to A12, P1. The remaining secondary winding of the toroidal transformer is connected to the bridge rectifier (CR3) that supplies raw dc power to the +5V supplies. One of these wires passes through an in-line fuse that protects the +5V logic power supply.

Table 5-2. *A12 Power Supply PCB Outputs*

Power Supply	Destination
+15V(A2)	A1/A2 Signal Channel Amplifier PCB A3 Signal Channel Interface PCB
–15V(A2)	A1/A2 Signal Channel Amplifier PCB A3 Signal Channel Interface PCB
+15V(A1)	A4 Sweeper Interface PCB
–15V(A1)	A4 Sweeper IF PCB
+12V	Fan & Monitor
+5V (D2)	A1/A2 Signal Channel Amplifier PCB A3 Signal Channel Interface PCB
+5V (D1)	A4 Sweeper IF PCB A8 GSP PCB A7 CPU PCB Front Panel A2 PCB

Note: A1, A2, D1, & D2 in Power Supply column indicate analog and digital voltages

Each of the seven power supply circuits includes a three-terminal power regulator integrated circuit. The output voltages of these power supplies are routed through connector P2 via a multi-wire cable harness to the A9 Motherboard PCB assembly. The A9 PCB distributes the power supply voltages to the various functions and PCBs within the instrument.

Polyswitches

Polyswitches RT1, RT2 and RT3 are temperature dependent resistors used as solid state fuses. They protect the instrument from any major circuit failure that might cause excessive transformer secondary current. These devices are wired in series with the secondary windings of the ±15V and +12V supplies.

Whenever the current flow through the polyswitch exceeds the threshold value, the polyswitch will change state and go into a high-resistance mode of operation. This automatically limits the current and protects the instrument. The polyswitch is reset by switching off the line power to the instrument and allowing it to return to normal temperature before re-applying power. (The fault that caused the over-current condition should be removed before the power is re-applied.)

Regulator Circuits

All of the 56100A power supplies use three-terminal variable set regulators that feature internal short circuit protection and over-temperature shut down operation. The linear regulator of each supply controls the output voltage of the supply to the specified voltage. The regulators are arranged in three banks, each bank being supplied from a different transformer secondary winding.

Regulator VR5 is the high current three-terminal regulator that is used to supply the +12V power for the dc fan and the Internal CRT Monitor assembly. AC power from the transformer secondary for this supply is connected to the A12 PCB via pins 2 and 3 of connector P1. One line is routed through polyswitch RT3 to the bridge rectifier CR2. The rectified voltage charges the reservoir capacitor C15.

The +12V output of VR5 is determined by the ratio of R12 and R13. Additional filtering for the set point is provided by C17. Diode CR13 protects the regulator from line hold up. Capacitors C16 and C18 provide the input and output filtering for the regulator

circuit. CR14 provides a fast discharge path for C17 if the output circuit is shorted.

Regulators VR6 and VR7 are configured similar to VR5 and are used to provide the +5V dc power to the instrument. The +5V power from VR6 is used for the digital PCBs, A5-A7 and A13. Two regulators are used instead of one, in order to distribute the power throughout the instrument more evenly and to reduce local loading effects.

Regulators VR1 and VR2 are used to control the +15V and -15V power supplies used for the signal channel PCBs A1, A2 and A3. Similarly, VR3 and VR4 are used to control the other ±15V supplies used with PCBs A4 through A7.

+5V Monitor LED

The +5V supply for the digital PCBs (regulator VR6) is provided with a LED indicator monitor circuit. This circuit is comprised of LED indicator CR19 and resistor R17 that are connected to the output of VR6.

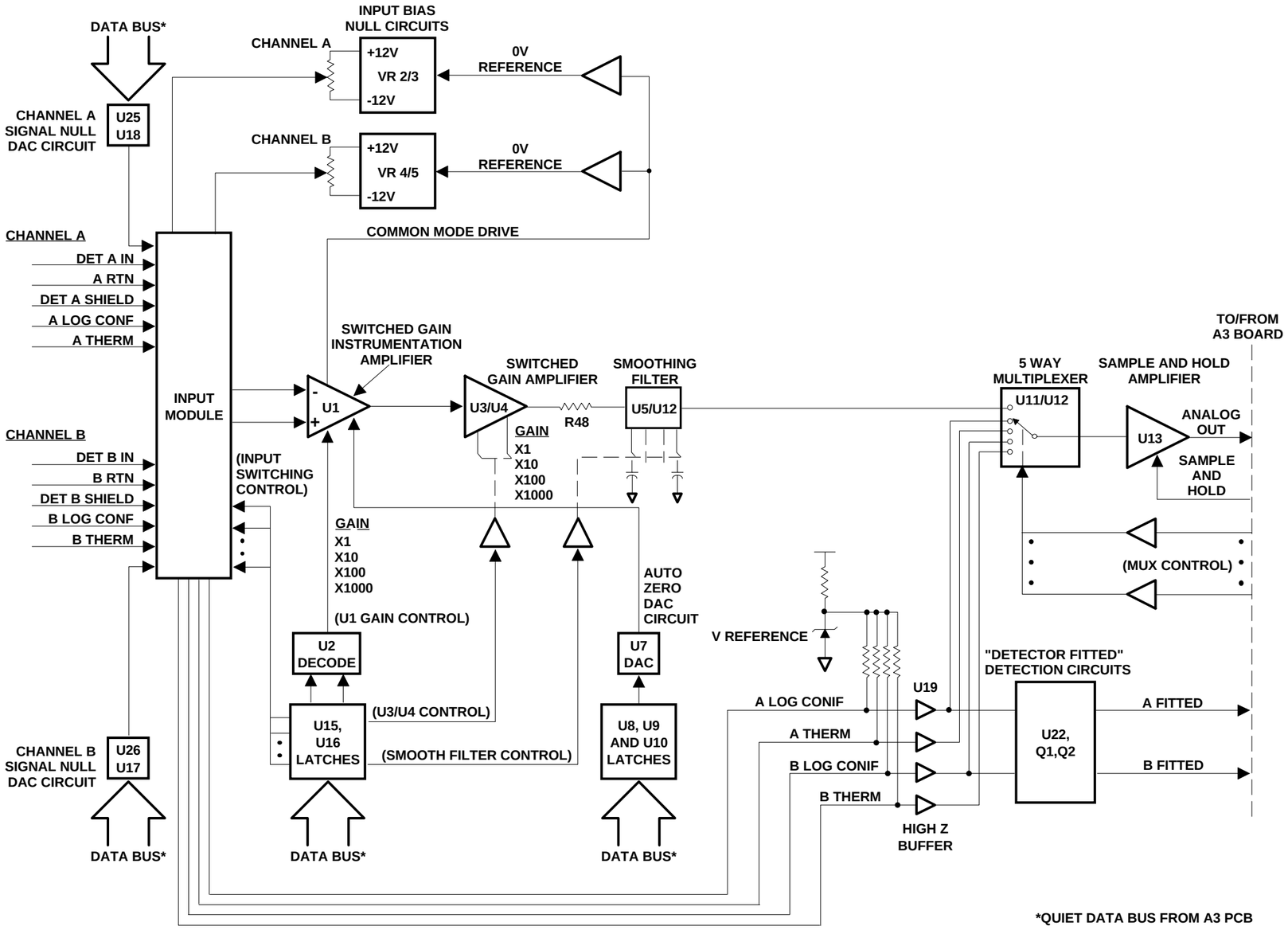

Figure 5-FO1. *Overall Block Diagram of A1/A2 Signal Channel Amplifier PCB*

Chapter 6
Removal and Replacement Procedures

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Chapter 6
Removal and Replacement Procedures

6-1 INTRODUCTION

The disassembly procedures presented in this chapter describe how to gain access to the major 56100A assemblies and parts for troubleshooting or replacement.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many assemblies in the 56100A contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-6.

6-2 REMOVE AND REPLACE 56100A COVERS

Adjustment and troubleshooting operations require removal of the top cover and removal of the PCB card clamp. Replacement of some 56100A assemblies and parts require removal of all covers. The following procedures describe this process. The replacement process is a reversal of the removal process.

Preliminary

☐ Disconnect the power cord from the unit.

Procedure

Step 1. To remove the top cover:

- Place the 56100A on its bottom (top-side up).
- Remove the feet from the two top corners at the rear of the 56100A (Figure 6-1).
- Remove the center screw from rear of the top cover.
- Lift and slide the top cover away from the 56100A.

Step 2. To remove the bottom cover:

- Place the 56100A on its top (bottom-side up).
- Remove the feet from the two bottom corners at the rear of the 56100A.
- Remove the center screw from rear of the bottom cover.
- Lift and slide the bottom cover away from the 56100A.

Step 3. To remove the left cover:

- Place the 56100A on its right side (left-side up).
- Remove the feet from the two left-side corners at the rear of the 56100A.
- Remove the center screw from rear of the left side cover.
- Lift and slide the side cover away from the 56100A.

Step 4. To remove the right cover (handle side):

- Place the 56100A on its left side (right-side up).

- Remove the feet from the two right-side corners at the rear of the 56100A.
- Remove the center screw from rear of the right side cover.
- Peel back the rubber sheathing at either end of the handle assembly, and remove the screws from underneath. Pull the handle straight away, and set it aside.
- Lift and slide the side cover away from the 56100A.

CAUTION

Screws with green heads have Metric threads.

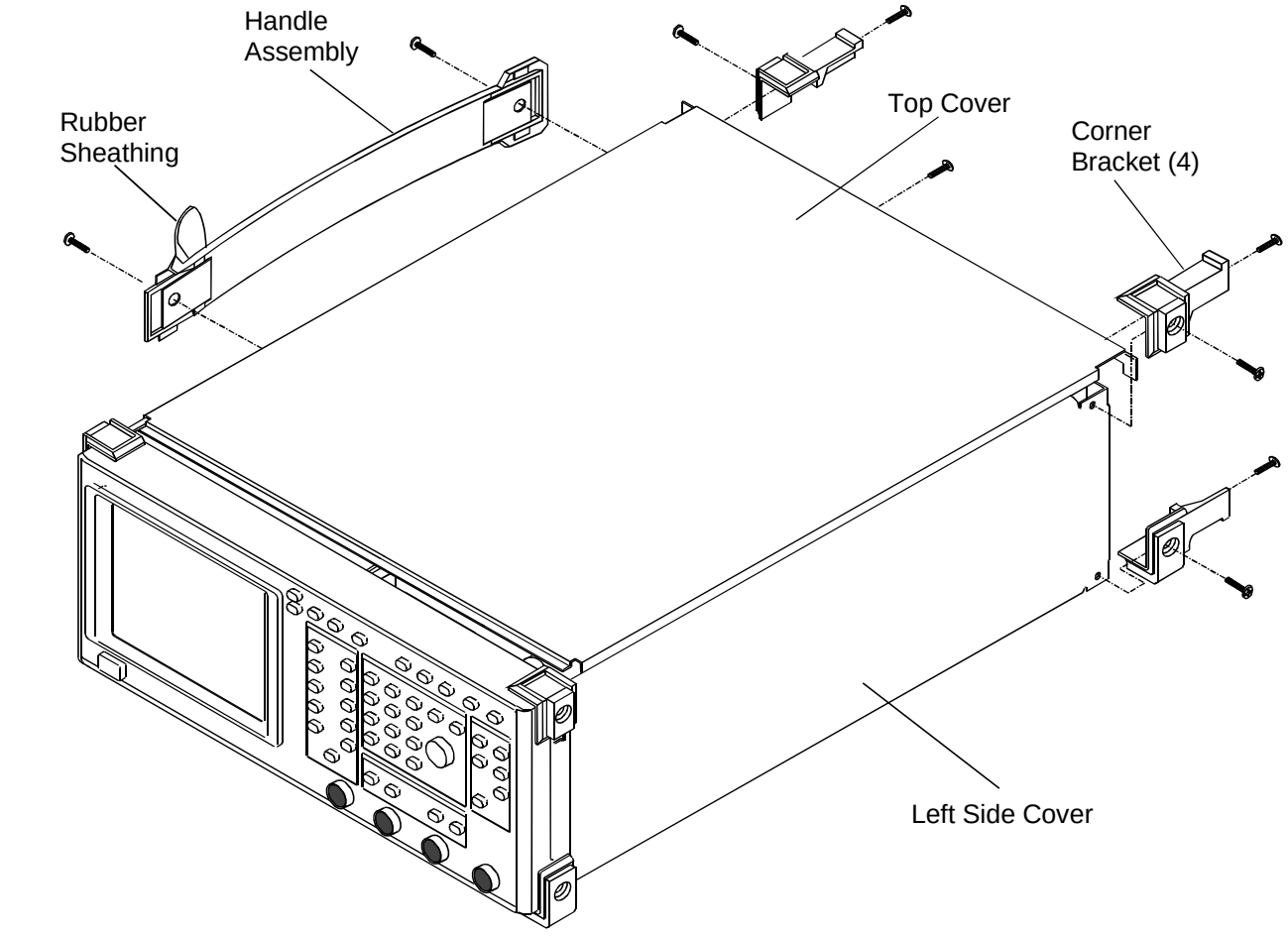

Figure 6-1. *Exploded View of Chassis Covers*

6-3 REMOVE AND REPLACE THE A1, A2, A3, A4, A7, AND A8 PCBs

This paragraph provides instructions for removing and replacing the A1, A2, A3, A4, A7, and A8 PCB's, which are located underneath the cover of the card cage. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top cover (paragraph 6-2).

Procedure

Step 1. Place the 56100A on its bottom (top-side up).

Step 2. Loosen the six captive screws on the card-cage cover (Figure 6-2).

Step 3. Remove card-cage cover and set aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight away. (Note that locations of PCB's are shown on top of card-cage cover.)

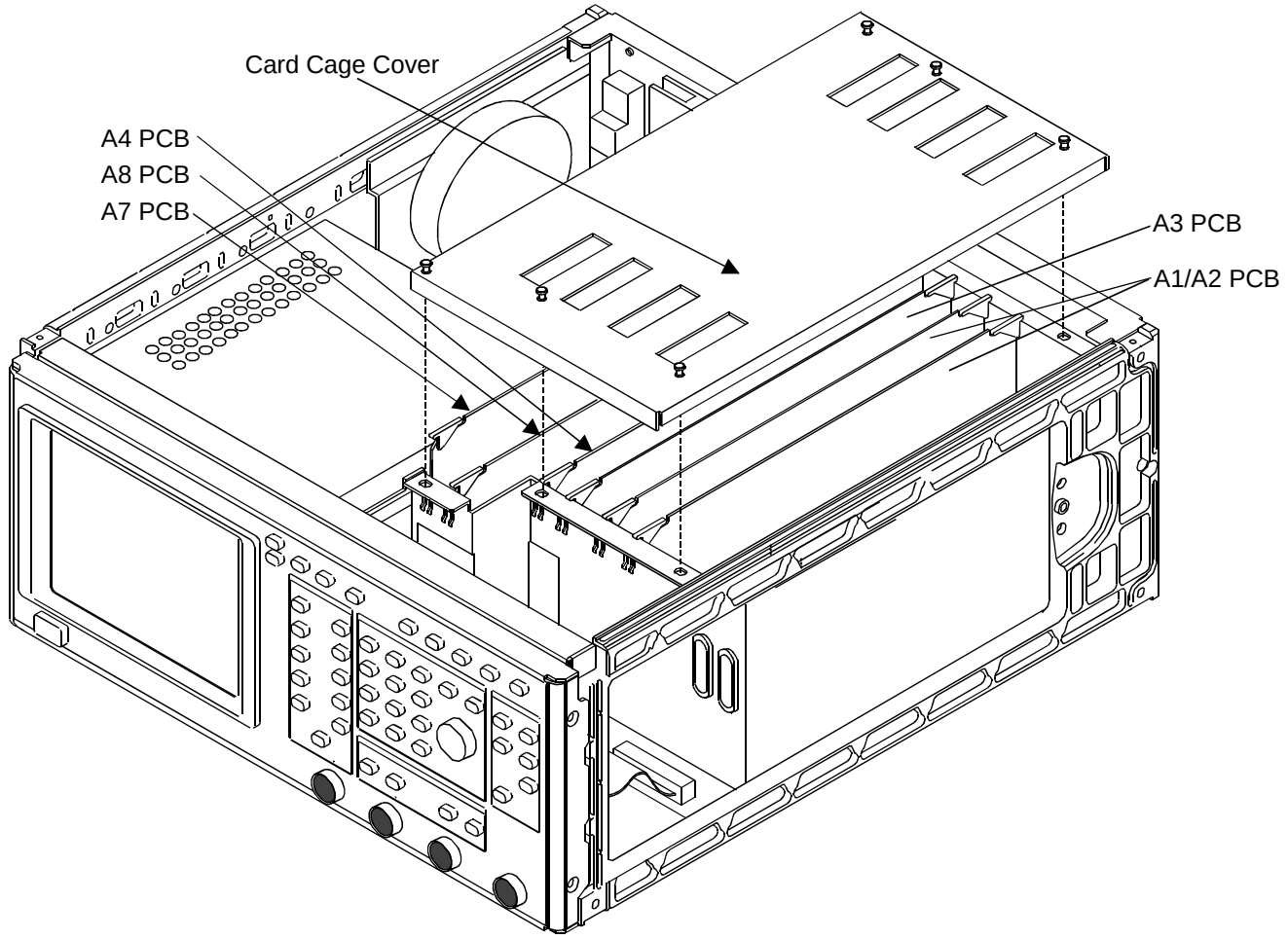

Figure 6-2. *Location of A1, A2, A3, A4, A7, and A8 PCBs*

6-4 REMOVE AND REPLACE THE FRONT PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the front panel assembly of the 56100A. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top, bottom, and side covers (paragraph 6-2).

Procedure

Step 1. Orient the 56100A as appropriate to remove the four corner brackets and tilt bail from the front of the 56100A (Figure 6-3).

Step 2. Slide the surrounding bezel straight away from the front panel, and set it aside.

Step 3. Remove two screws from the bottom of the front panel and pull out the Power On/Off switch (leave wires connected).

Step 4. Remove screw from center bottom of front panel.

Step 5. Place the 56100A on its side (PCB side up).

Step 6. Disconnect the ribbon cable from connector J1 on the front panel interface PCB by pulling it straight away.

Step 7. Remove the ground wire from the side frame by unscrewing the securing nut.

Step 8. Carefully remove connectors from P1 and P2 on A1 and A2 PCBs.

Step 9. Remove cable clamp holding A1 and A2 cables to housing.

Step 10. Place the 56100A on its bottom (top-side up).

Step 11. Remove the four side screws and gently pull front panel assembly forward to remove.

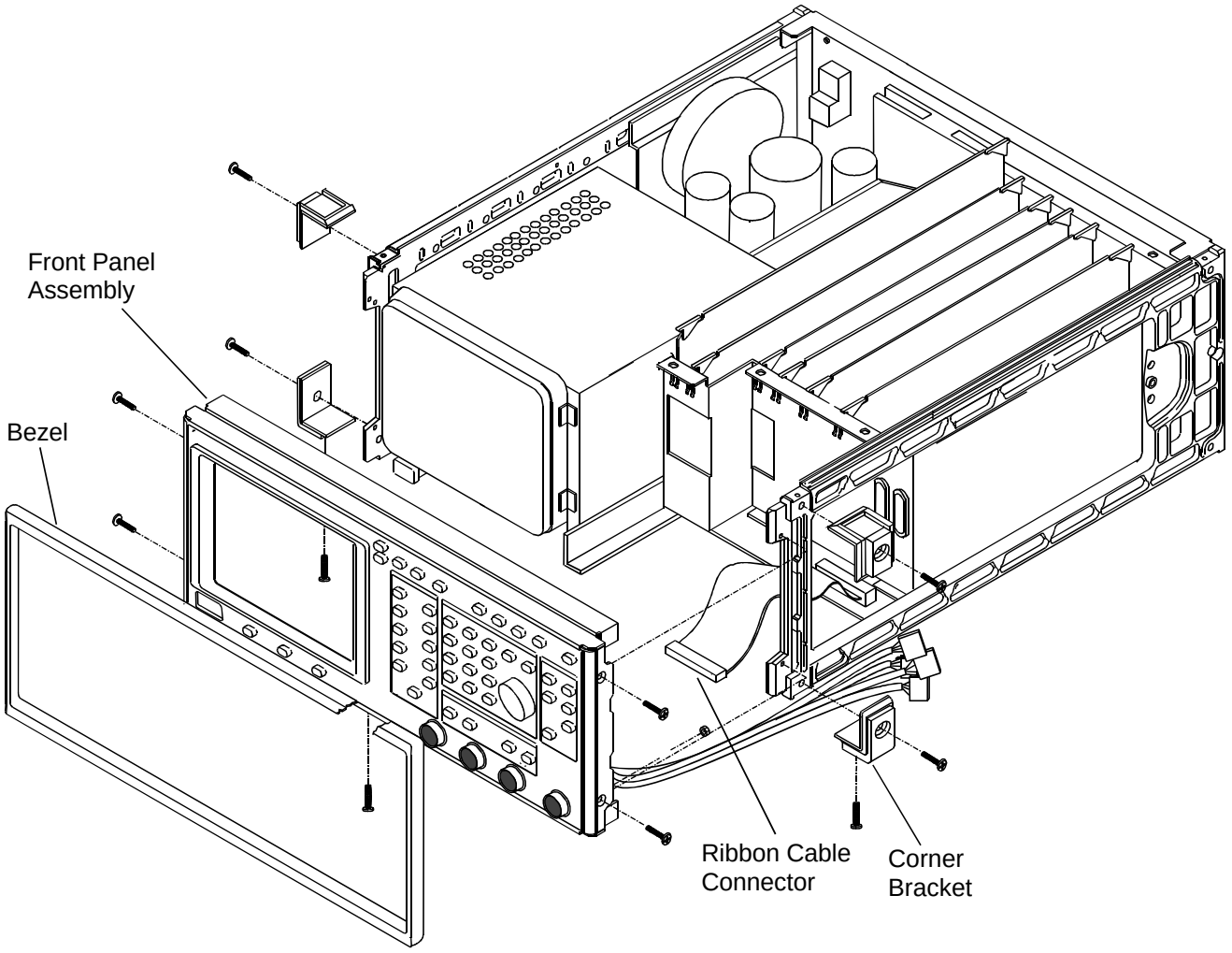

Figure 6-3. *Exploded View of Front Panel Assembly*

6-5 REMOVE AND REPLACE THE A1/A2 PCB

This paragraph provides instructions for removing and replacing the A2 Front Panel Interface PCB. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top, bottom, and side covers (paragraph 6-2).

☐ Remove the front panel assembly (paragraph 6-4).

Procedure

Step 1. Diconnect the cable from the front panel motor to the A2 front panel interface PCB.

Step 2. Remove eight screws that secure PCB (Figure 6-4).

Step 3. Remove the A1 and A2 PCBs by lifting them straight away. Carefuly separate the two PCBs.

6-6 REMOVE AND REPLACE THE FRONT PANEL KEY SWITCH MEMBRANE

This paragraph provides instructions for removing and replacing the front panel keys switch membrane. The replacement process is a reversal of the remove process.

Preliminary

☐ Remove the top, bottom, and side covers (paragraph 6-2).

☐ Remove the front panel assembly (paragraph 6-4).

☐ Remove the A1/A2 PCB assembly (paragraph 6-5).

Procedure

Step 1. With the key-switch membrane exposed, carefully peel it away from the inside of the front panel backplate (Figure 6-4, Detail A).

CAUTION

Avoid touching the black switch contacts in the membrane. They can be damaged or destroyed by the oils in human skin.

NOTE

A metal screen shrouds the in/out connector PCB assembly. It is held in place by two screws that screw in to the front panel assembly. The screen can be removed either when the front panel is connected to the unit or after it is removed.

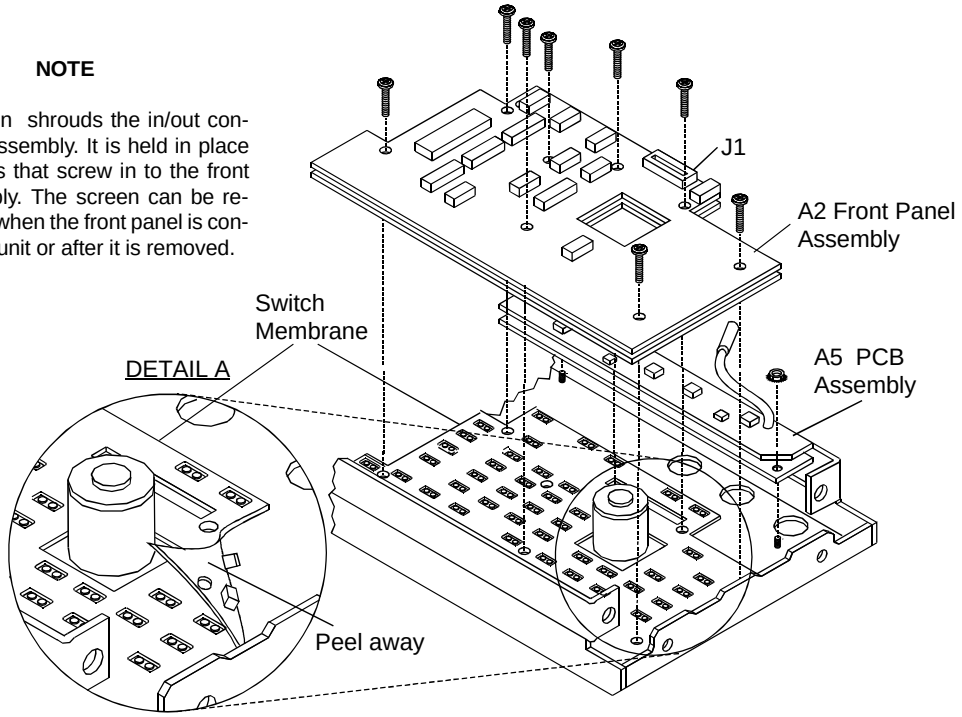

Figure 6-4. *Exploded View of A1, A2, and A5 PCBs*

6–7 REMOVE AND REPLACE THE A5 PCB

This paragraph provides instructions for removing and replacing the A5 Signal Channel Connectors PCB. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top, bottom, and side covers (paragraph 6-2)

☐ Remove the front panel assembly of the unit (paragraph 6-4).

Procedure

Step 1. Remove the input connector PCB metal screen from the front panel metal work by removing the two mounting screws.

Step 2. Disconnect the chassis ground wire (yellow and green wire from the Input Connector PCB) from the side frame by removing the securing nut.

Step 3. Remove five nuts, and lift the A5 PCB straight away (Figure 6-4).

6-8 REMOVE AND REPLACE THE POWER SUPPLY ASSEMBLY

This paragraph provides instructions for removing and replacing the Power Supply Assembly, which consists of the A9 Power Supply Motherboard PCB and the toroidal transformer. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top, bottom, and side cover on power supply side (paragraph 6-2).

Procedure

Step 1. Place 56100A on its right side (power supply side up).

Step 2. Remove two screws from the Line Power Input connector (Figure 6-5).

Step 3. Pull connector from hole and disconnect wires (spade connectors) leading to power supply.

Step 4. Disconnect power supply ground wire at chassis.

Step 5. Disconnect cable connector leading from unit motherboard at power supply PCB.

Step 6. Remove six screws that fasten power supply PCB assembly to chassis (Figure 6-5).

Step 7. Remove two nuts that fasten power supply toroidal transformer to chassis (Figure 6-5).

Step 8. Lift power supply PCB assembly and transformer from unit.

Step 9. Reassemble in the reverse order. Refer to Table 6-1 and Figure 6-7 (page 6-16) for the color coded connections to the Line Power Input connector.

Table 6-1. *Line Power Input Connector Pin Designation*

CONNECTOR PIN	WIRE COLOR
A	White
B	Brown
C	Purple
D	Red
E	Pink
F	Blue
G	Brown

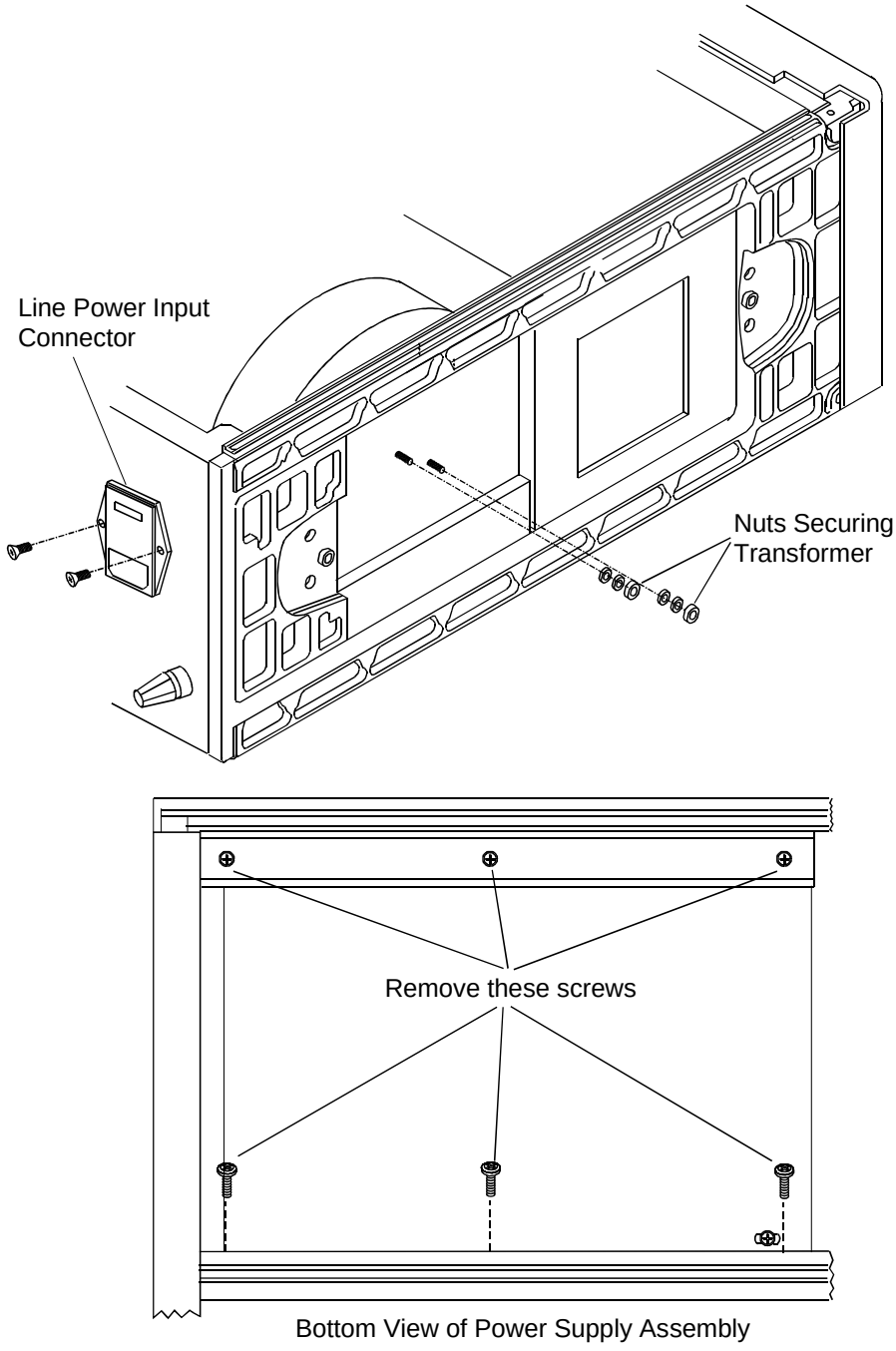

Figure 6-5. *Power Supply Removal*

6-9 REMOVE AND REPLACE THE CRT MONITOR ASSEMBLY

This paragraph provides instructions for removing and replacing the CRT Monitor Assembly, which consists of the CRT monitor unit and mounting bracket. The CRT Monitor Assembly is removed/ replaced as a complete unit. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top and bottom covers (paragraph 6-2).

☐ Remove the A7 and A8 PCBs (paragraph 6-3).

Procedure

Step 1. Place the 56100A on its side (CRT side up).

Step 2. Disconnect the CRT monitor assembly cable at connector J2 on the Motherboard PCB.

Step 3. Remove four screws, flat, and lock washers (Figure 6-6).

Step 4. While supporting the CRT monitor assembly, place the 56100A on its bottom side (top-side up).

Step 5. Move the assembly to the rear and lift from unit.

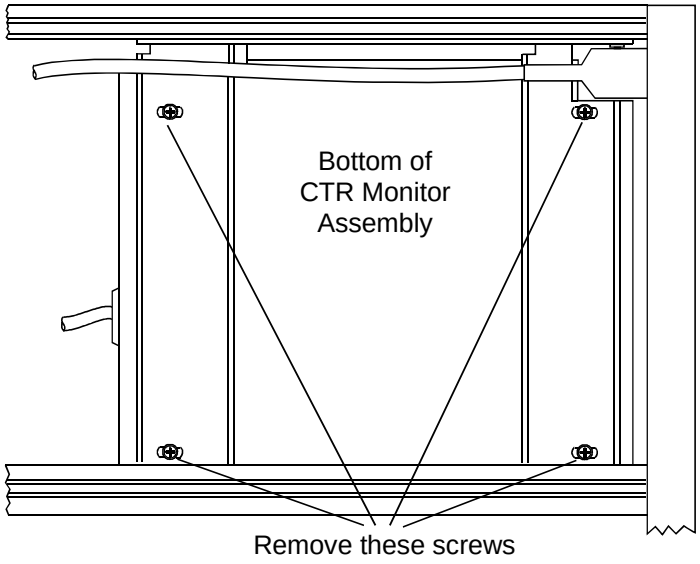

Figure 6-6. *CRT Removal*

6-10 REMOVE AND REPLACE THE REAR PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the Rear Panel Assembly. This panel must be removed to replace the rear panel connectors. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top, bottom, and side covers (paragraph 6-2).

Procedure

Step 1. Remove the screw from the bottom center of the rear panel.

Step 2. Place unit on bottom (top side up) and remove ribbon cable connector from A7 PCB.

Step 3. Carefully remove one screw from the middle of either side of the rear panel (Figure 6-7).

Step 4. Tilt rear panel to gain access to connectors on motherboard.

Step 5. Remove three connectors from motherboard.

Step 6. Remove wires (spade connectors) from the Line Power Input connector.

NOTE

When replacing rear panel, refer to Table 6-1 for the color coded wiring connections at the Line Power Input connector.

Step 7. Remove wires from chassis ground connection.

Step 8. Lift the rear panel away from the frame to remove.

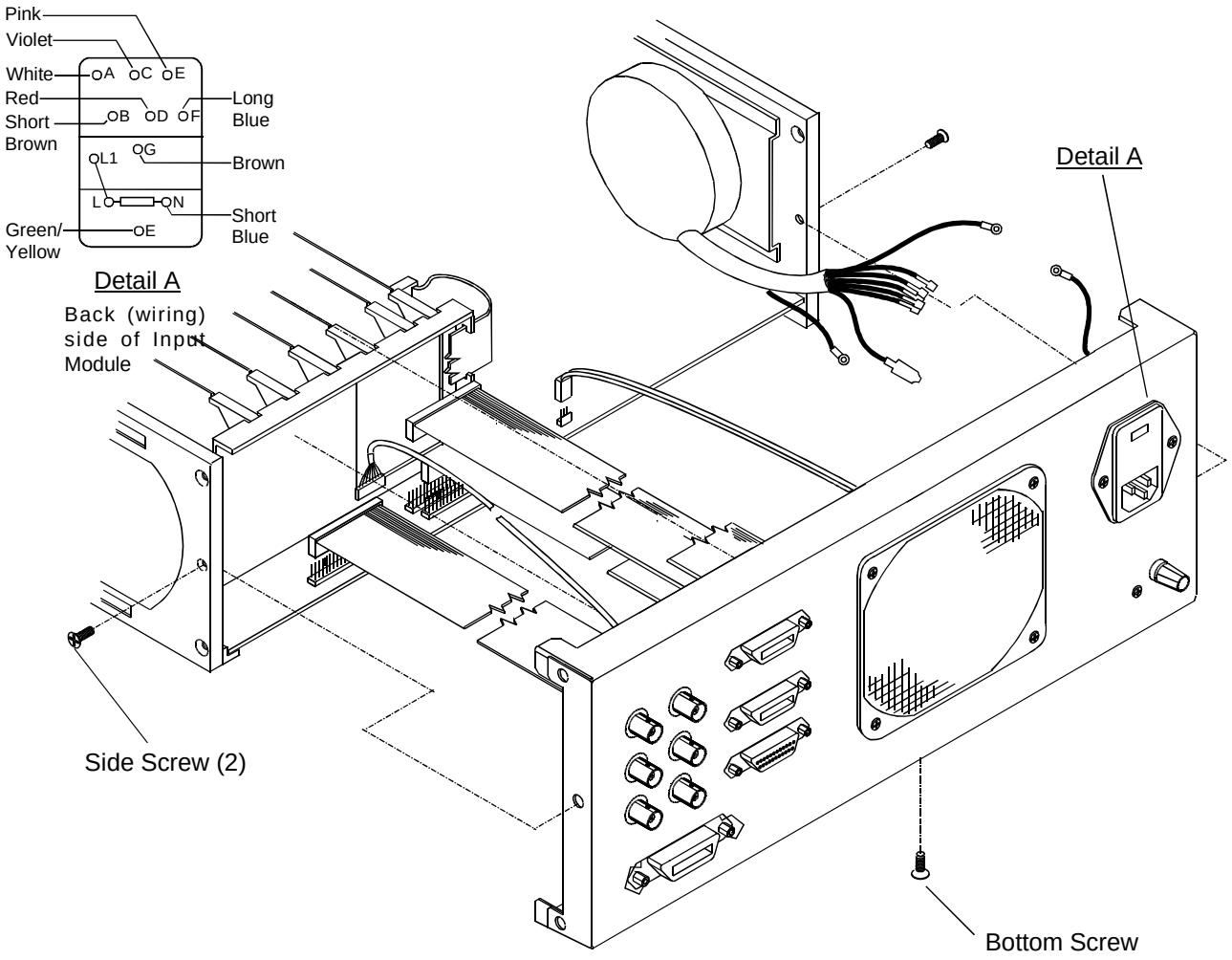

Figure 6-7. *Rear Panel Removal*

6-11 REMOVE AND REPLACE THE COOLING FAN ASSEMBLY

This paragraph provides instructions for removing and replacing the rear panel cooling fan assembly. The replacement process is a reversal of the removal process.

Preliminary

☐ Remove the top cover (paragraph 6-2).

Procedure

Step 1. While supporting the fan from the backside, remove four corner screws and pull the fan guard straight away (Figure 6-8).

IMPORTANT NOTE
Do not remove the fan just for cleaning. Clean it in place using a brush or a vacum cleaner.

Step 2. Carefully lift and rotate fan assembly to gain access to the fan connector on the motherboard. Remove connector.

Step 3. Lift the fan away from the unit.

NOTES

- The fan has four metal spring mounting clips that have to be removed. Re-use when fitting a new fan or re-fitting the original fan.
- Install the fan connection on the motherboard before reassembling the fan to the rear panel.
- The fan guard should be cleaned at this time, if necessary.

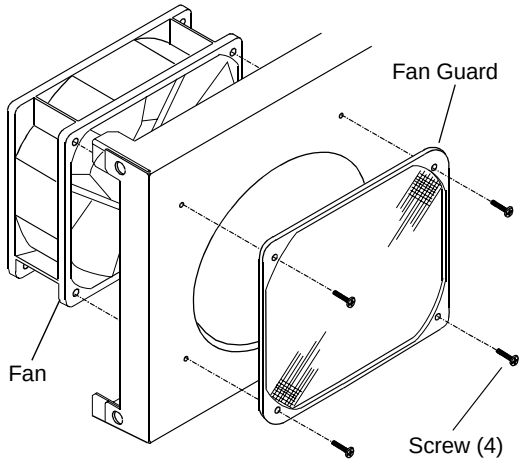

Figure 6-8. *Exploded View of Cooling Fan Assembly*

Appendix A
RF Detector Diode Replacement Procedures

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Appendix A
RF Detector Diode Replacement Procedures

A-1 RF DETECTOR DIODE REPLACEMENT PROCEDURES

Series 5400-71XXX RF Detectors and series 560-7XXX RF Detectors are used with 56100A SNA. Paragraph A-2 contains the procedure for replacing defective detector diodes in model 5400-71B75 RF Detectors, and paragraph A-2 contains the procedure for replacing detector diode modules in series 560-7XXX RF Detectors.

NOTE

Models 5400-71N50 and 5400-71N75 RF Detectors do not have field-replaceable detector diodes. Series 5400-6NXXX Autotesters also do not.

Required Adjustments

Whenever the detector diode (or diode module) of these RF Detectors is replaced, the two potentiometers that are part of the rf detector PCB subassembly (Figures A-1 and A-4) must be readjusted. The potentiometer readjustment is done after the defective diode is removed, but before the replacement diode is installed.

Test Equipment Required

The procedure in this appendix require a digital multimeter (DMM) that has a display resolution of at least 3-1/2 digits. (John Fluke Model 8840A, or equivalent).

A-2 REPLACEMENT OF DETECTOR DIODE FOR MODEL 5400-71B75 RF DETECTOR

The model 5400-71B75 RF Detector is equipped with a field-replaceable detector diode. To replace, proceed as follows:

Step 1 Unfasten the four detector housing top cover retaining screws. Remove the top cover.

Step 2 Unplug the defective diode (Figure A-1) from the PCB subassembly and remove.

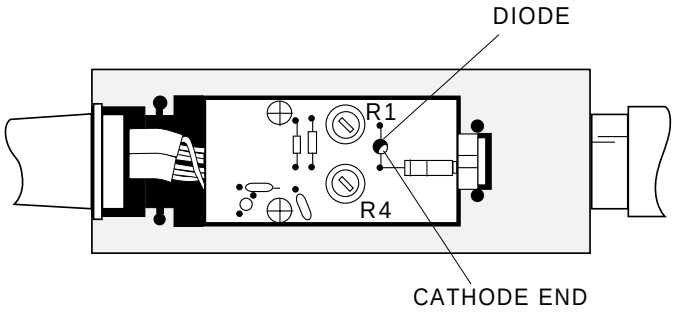

Figure A-1. *Model 5400-71B75 RF Detector Housing Layout Diagram*

Step 3 Set potentiometer R1 fully clockwise (maximum resistance).

Step 4 Connect the DMM leads between pins 1 and 2 of the RF detector cable connector (Figure A-2). Measure the resistance value, which is the maximum resistance of R1 (approximately 40.5 kΩ is typical). Record this value; it will hereafter be referred to as "R_T".

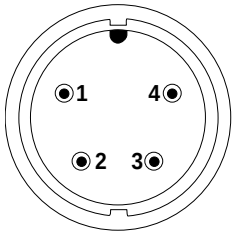

Figure A-2. *RF Detector Cable Connector Pin Orientation*

Step 5 Obtain the "K" value from the replacement diode container label (Figure A-3).

Step 6 Compute the set value for R1 as follows:

$$R1_{set} = K \times R_T$$

Step 7 Adjust R1 counterclockwise until the DMM indicates the $R1_{set}$ value calculated in step 6.

Step 8 Connect the DMM leads between pin 3 of the rf detector cable connector and the cable shield.

Step 9 Obtain the "R_0" value from the replacement diode container label.

Step 10 Adjust R4 until the DMM indicates the "R_0" value. Disconnect the DMM.

Step 11 Orient the cathode end (white dot) of the replacement diode as shown in Figure A-1 (white dot toward centerline of the detector PCB subassembly). Insert the diode into the socket of the PCB subassembly.

Step 12 Reinstall the top cover, securing it with the four retaining screws. This completes replacement of detector diode.

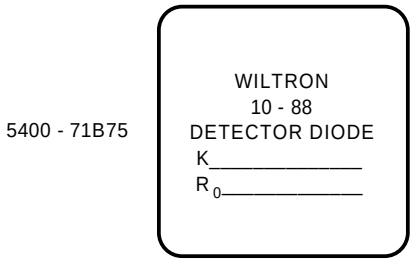

Figure A-3. *Replacement Diode Container Label*

A-3 REPLACEMENT OF DIODE MODULES FOR SERIES 560-7XXX RF DETECTORS

Series 560-7XXX RF Detectors are equipped with a field-replaceable diode module that contains (in addition to the detector diode) a thermistor, a resistor, and two capacitors. To replace, proceed as follows:

Step 1 Unfasten the four detector housing top cover retaining screws. Remove the top cover.

Step 2 Unfasten the two retaining screws that hold down the rf detector PCB subassembly (Figure A-4).

Step 3 Slide the cable retainer out of the rf detector housing assembly. When the cable retainer clears the housing, disconnect the PCB subassembly from the diode module. Remove spring washer.

Step 4 Remove fiberglass module retainer from detector housing. This retainer can be removed by prying it out using a small screwdriver, or by pulling it out using short, round nose pliers.

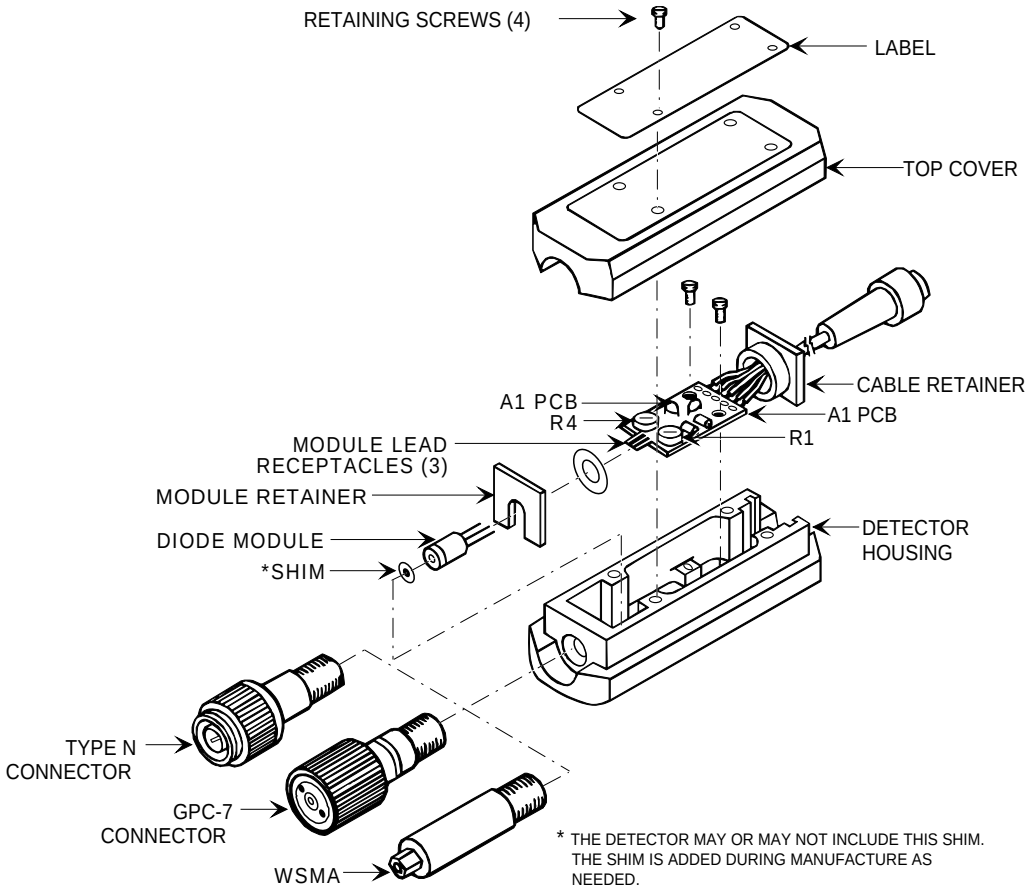

Figure A-4. *Series 560-7XXX RF Detectors, Exploded View*

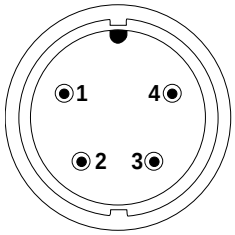

Figure A-5. *RF Detector Cable Connector Pin Orientation*

Step 5 Remove diode module from rear of connector body by pulling it straight out.

Step 6 Connect the DMM leads between pins 1 and 2 of the RF detector cable connector (Figure A-5). Measure the resistance value, which is the maximum resistance of R1 (approximately 40.5 kΩ is typical). Record this value; it will hereafter be referred to as "R_T".

Step 7 Obtain the "K" value from the replacement diode container label (Figure A-6).

Step 8 Compute the set value for R1 as follows:

$$R1_{set} = K \times R_T$$

Step 9 Adjust R1 counterclockwise until the DMM indicates the $R1_{set}$ value calculated in step 8.

Step 10 Connect the DMM leads between pin 3 of the rf detector cable connector and the cable shield.

Step 11 Obtain the "R_0" value from the replacement diode container label and adjust R4 until the DMM indicates this value. Disconnect the DMM.

Step 12 Orient detector housing normally (Figure A-4). Insert replacement diode module into rear of connector body so that center lead *is on top*.

Step 13 Orient spring washer so that the two curved flanges point toward the rear of the detector housing and are positioned horizontally (i.e., 3 o'clock and 9 o'clock positions).

Step 14 Insert fiberglass module retainer between the replacement diode module and spring washer. Push down on retainer until fully seated.

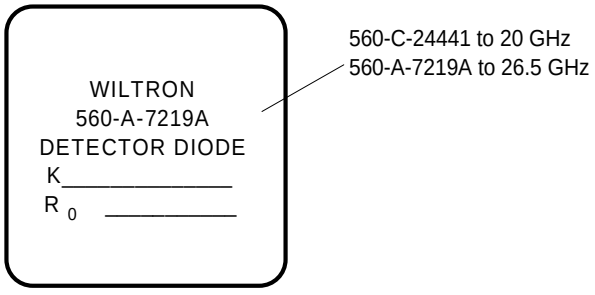

Figure A-6. *Replacement Diode Module Container Label*

Step 15 Orient PCB subassembly normally as shown in Figure A-4 and insert into detector housing so that leads from replacement diode module mate with connectors on PCB subassembly.

Step 16 Insert cable retainer into slot in detector housing.

Step 17 Fasten PCB subassembly into detector housing using two retaining screws.

Step 18 Reinstall the top cover, securing it with the four retaining screws. This completes replacement of detector diode module.

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